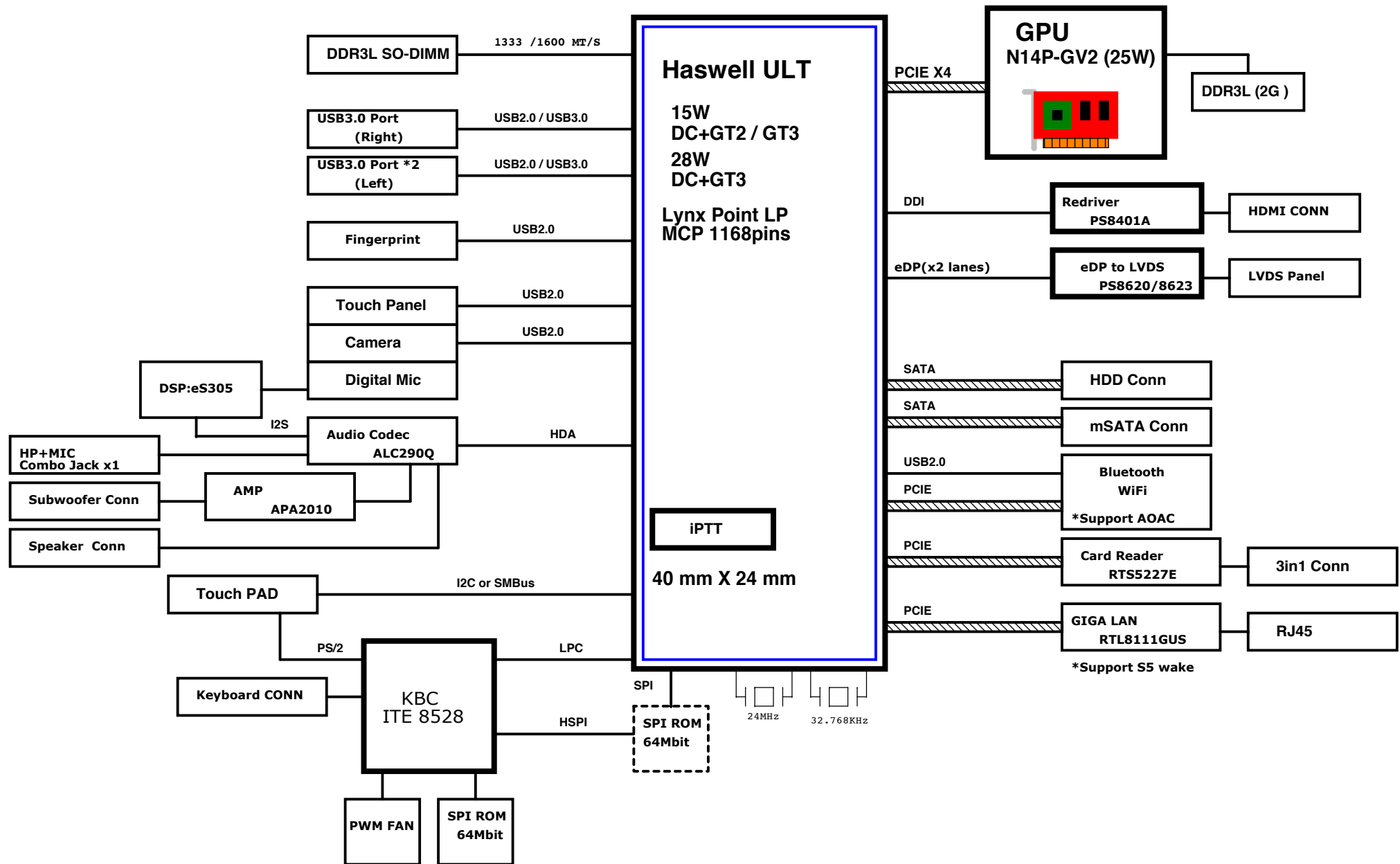


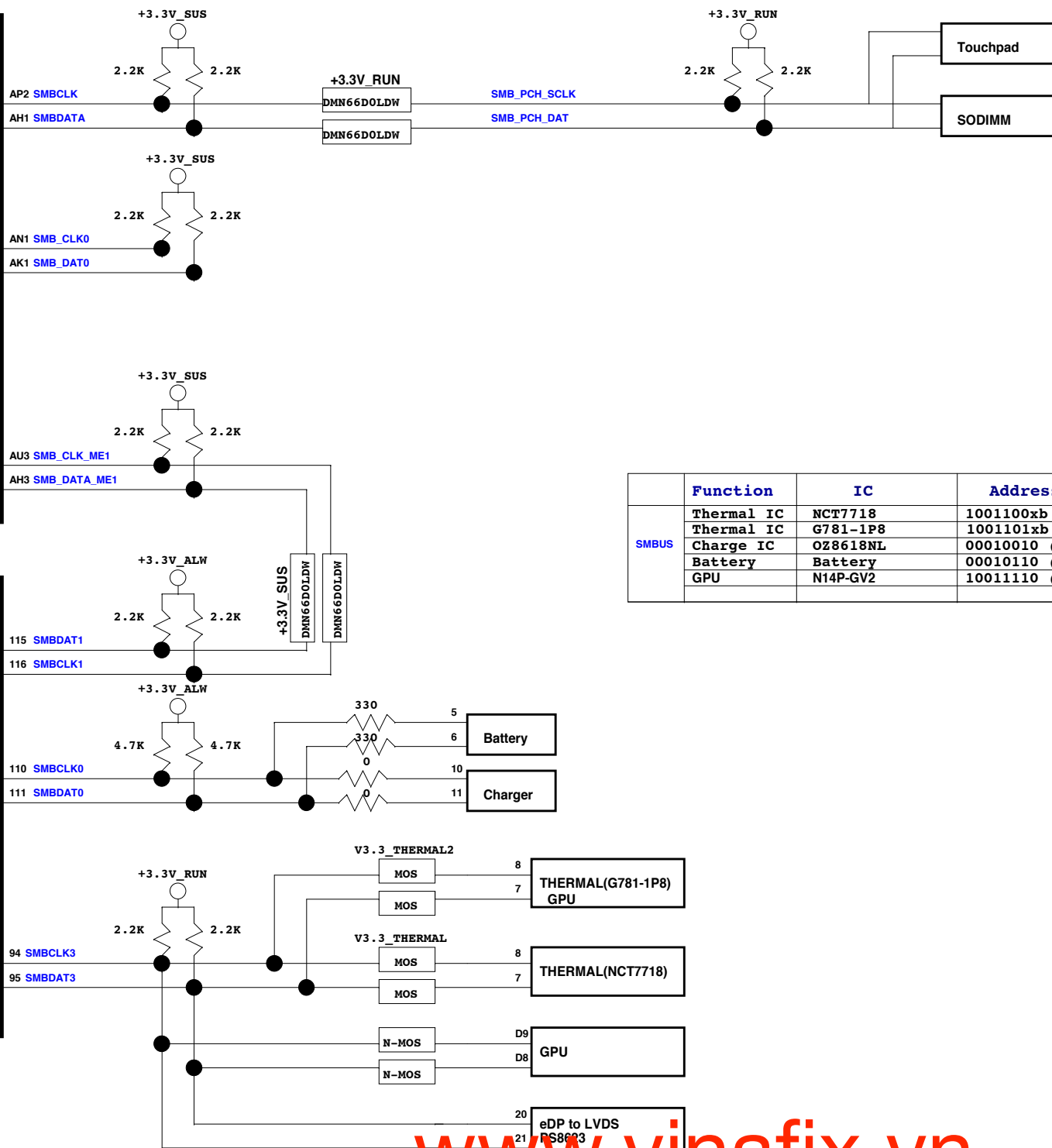
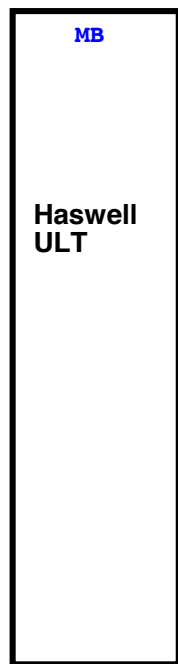
JW8B/C BLOCK DIAGRAM



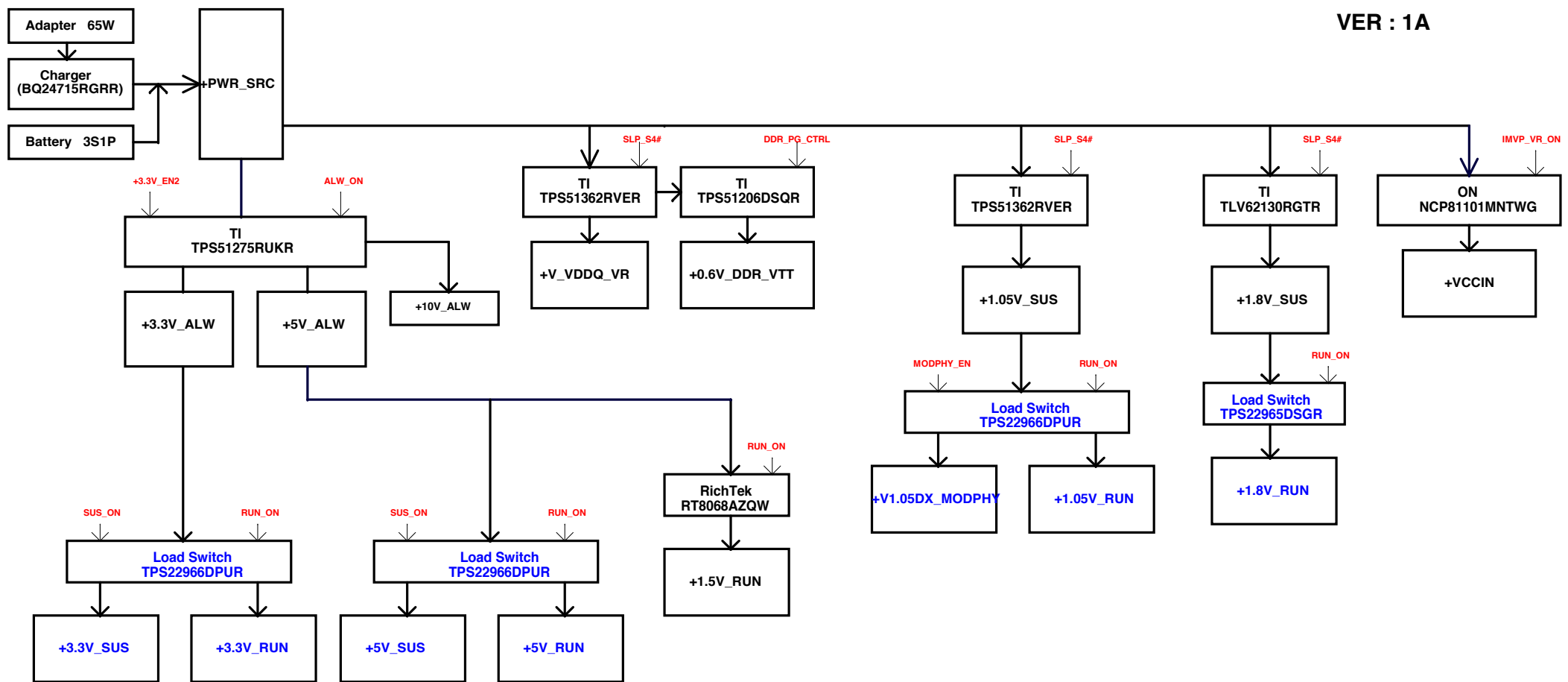
HSIO Port	USB3.0	PCIE	SATA
1	USB3.0_1 CN6		
2	USB3.0_2 CN4		
3	USB3.0_3 CN5	PCIE1 X	
4	USB3.0_4 X	PCIE2 Card Reader	
5		PCIE3 GIGA LAN	
6		PCIE4 WIFI	
7		PCIE5 GPU 4X	
8		PCIE5 GPU 4X	
9		PCIE5 GPU 4X	
10		PCIE5 GPU 4X	
11		PCIE6 X	SATA3 X
12		PCIE6 X	SATA2 mSATA
13		PCIE6 X	SATA1 HDD
14		PCIE6 X	SATA0 X

PCIE CLK
CLK0 X
CLK1 Card Reader
CLK2 GIGA LAN
CLK3 WIFI
CLK4 GPU 4X
CLK5 X

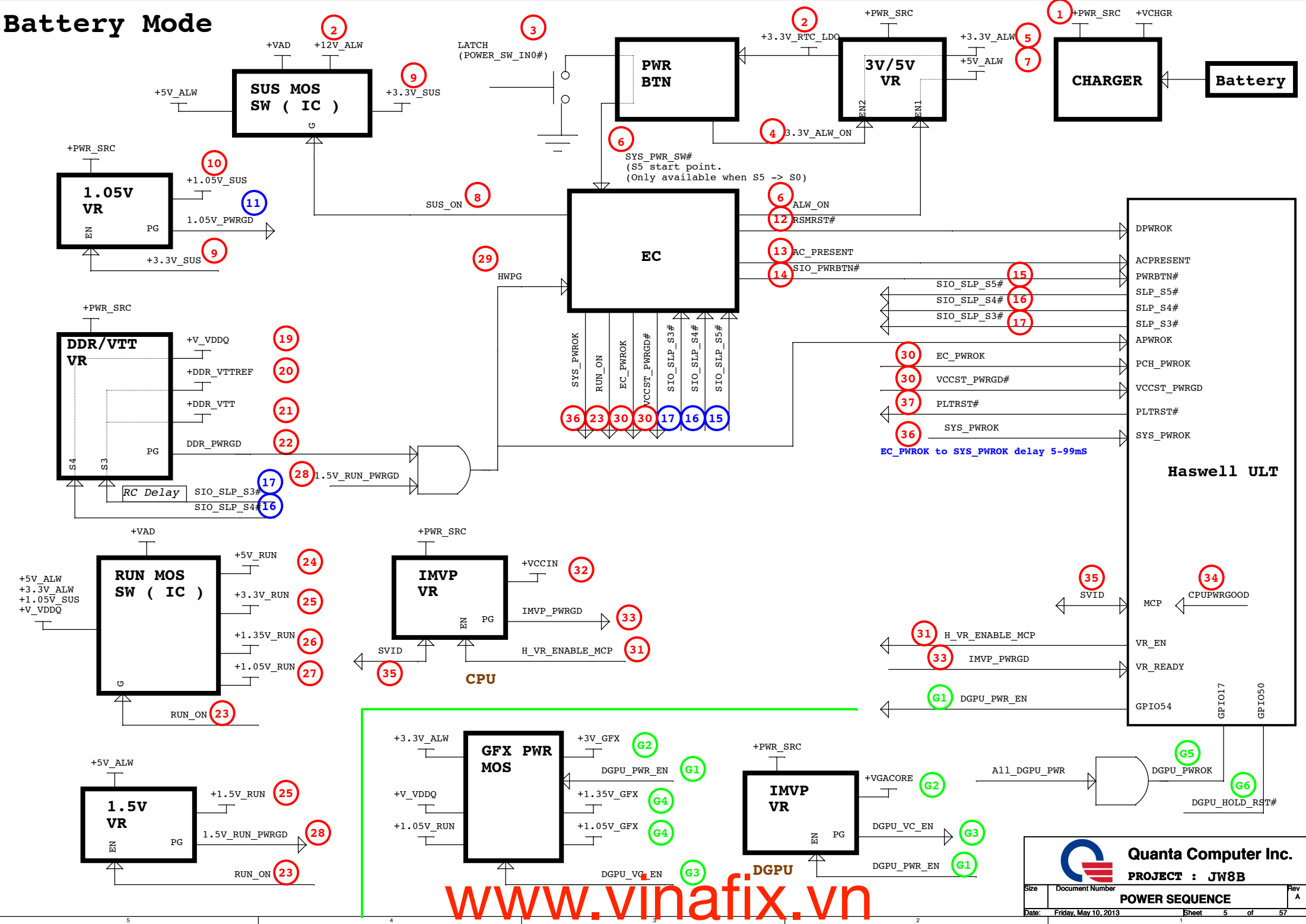
USB2.0
USB2.0_0 CN4
USB2.0_1 CN6
USB2.0_2 CN5
USB2.0_3 Finger Print
USB2.0_4 Camera
USB2.0_5 eTP
USB2.0_6 Blue Tooth
USB2.0_7 Touch Screen



	Function	IC	Address
SMBUS	Thermal IC	NCT7718	1001100xb (98h)
	Thermal IC	G781-1P8	1001101xb (9Ah)
	Charge IC	OZ8618NL	00010010 (0x12h)
	Battery	Battery	00010110 (0X16h)
	GPU	N14P-GV2	10011110 (0X9Eh)

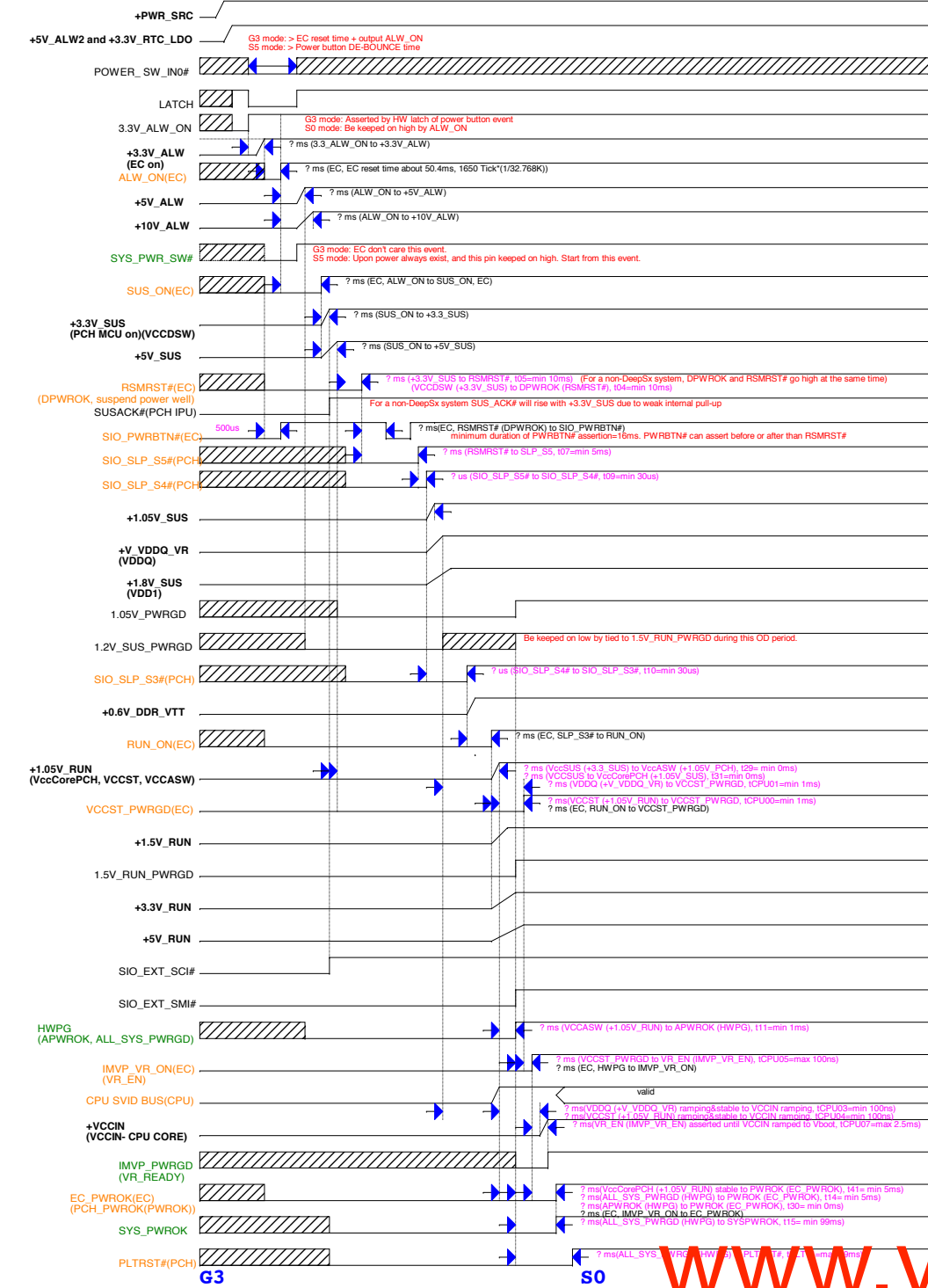


Battery Mode



Power Sequence
(G3 to S0)

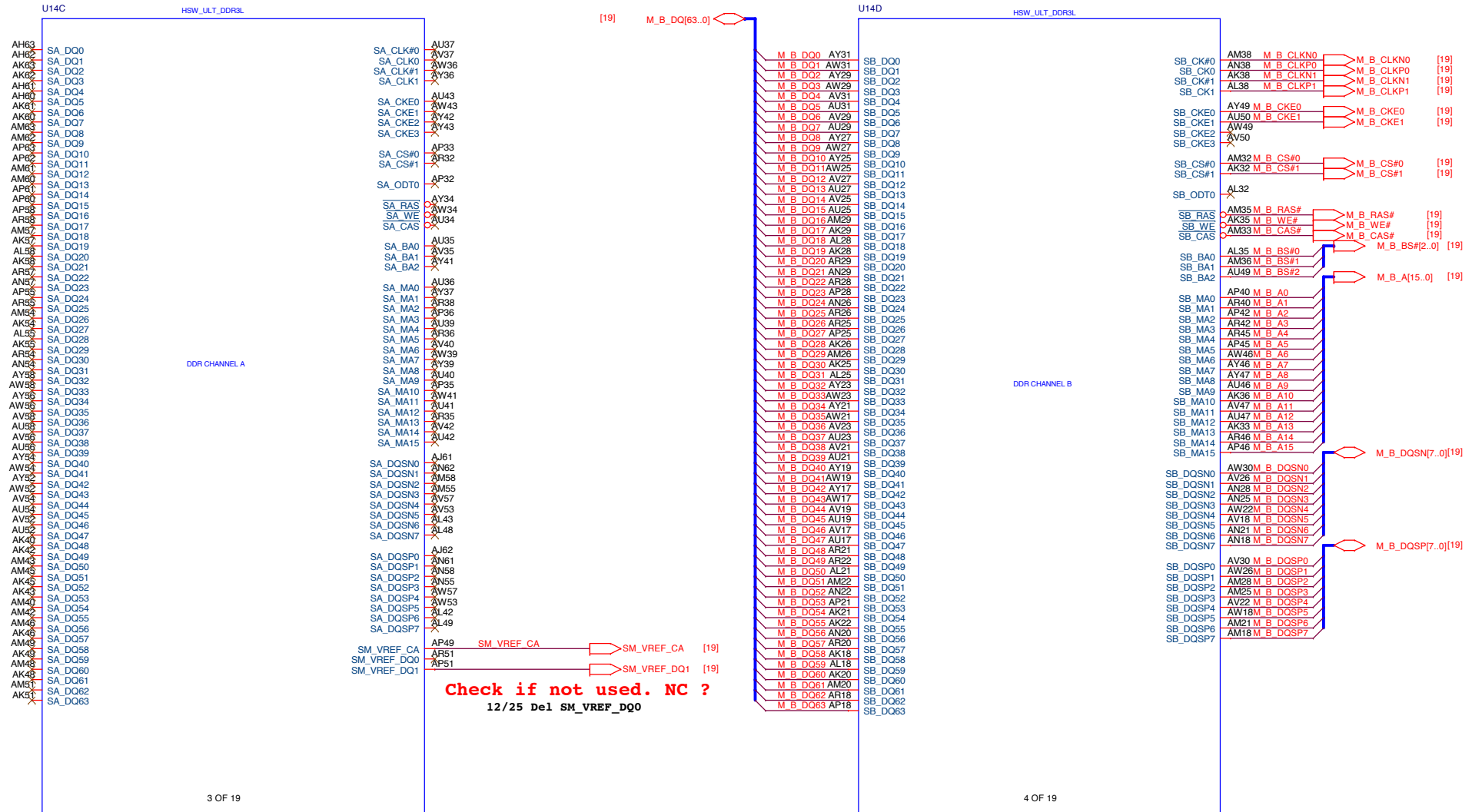
Shark Bay ULT PSS, 490828, Rev1.1



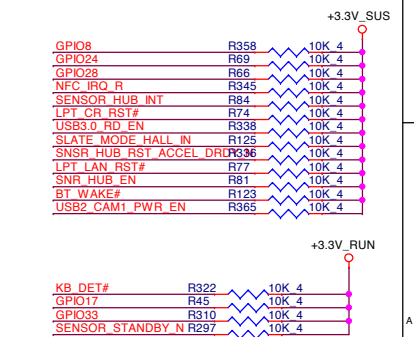
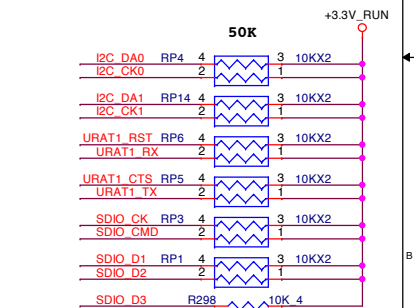
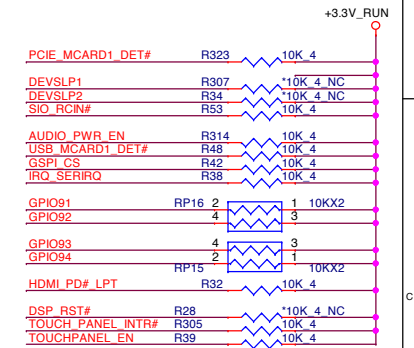
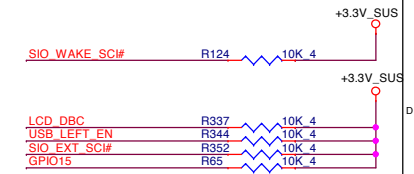
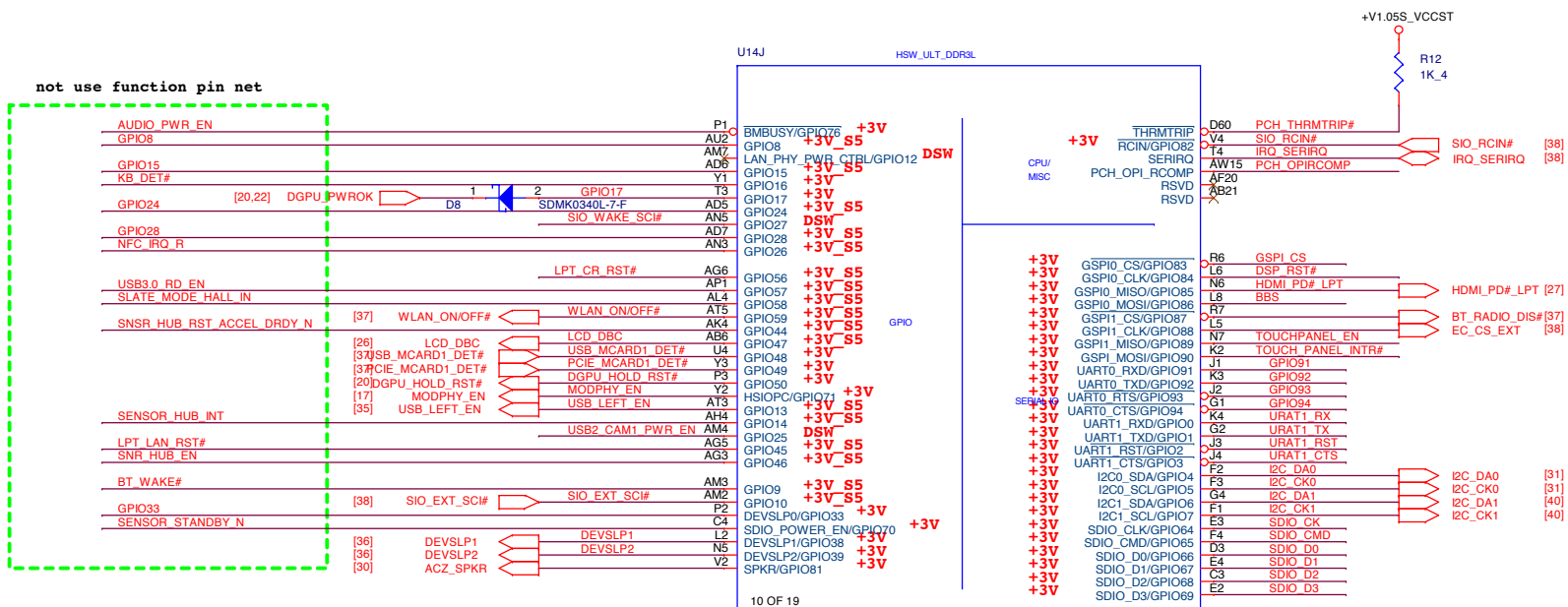
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Size	Document Number	Rev
	Haswell ULT 1/12	A
Date:	Tuesday, July 16, 2013	Sheet 7 of 57

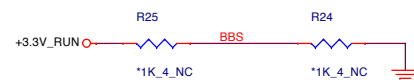
Haswell ULT (DDR3L)

GPIO Pull-up/Pull-down(CLG)



No Reboot Strap(GPIO81)	
NC	Default
PU	EN

GPIO86:Boot BIOS Strap Bit	
PU	LPC
PD	SPI (Default IPD)



TLS CONFIDENTIALITY STRAP(GPIO15)	
NC	Default
PU	EN

GPIO66 : Top-Block Swap	
R1547	ENABLE
R1547_NC	DISABLE(Default)



Haswell ULT (PCIE,USB)

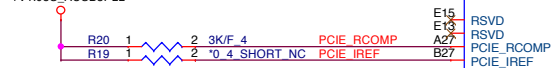
U14K

HSW_ULT_DDR3L

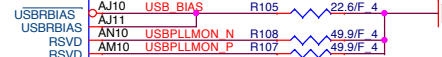
PCIE

USB

+V1.05S_AUSB3PLL



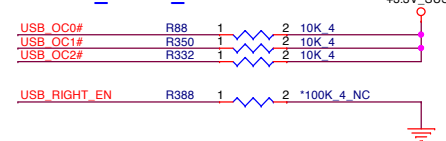
+3V_S5
+3V_S5
+3V_S5
+3V_S5



AL3 USB_OC0#
AT1 USB_OC1#
AH2 USB_OC2#
AV3 USB_RIGHT_EN

USB_OC0#
USB_OC1#
USB_OC2#
USB_RIGHT_EN[34]

HARRIS_BEACH_CS REV 3.0

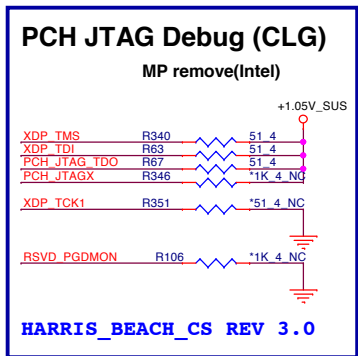
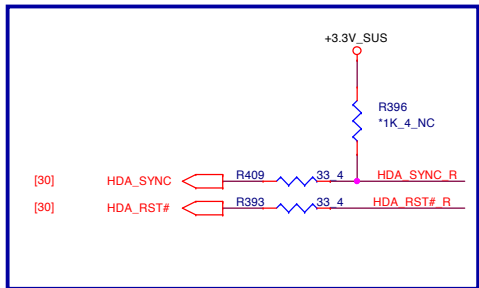
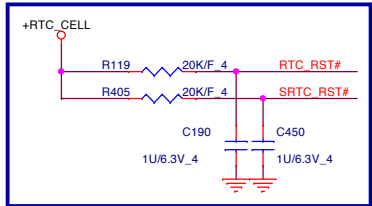
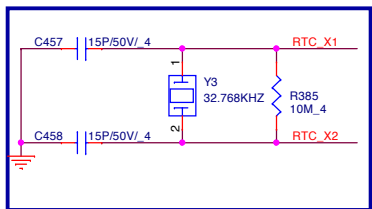


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Quanta Computer Inc.
PROJECT : JW8B

Size	Document Number	Rev
	Haswell ULT 4/12	A
Date:	Monday, July 08, 2013	Sheet 10 of 57

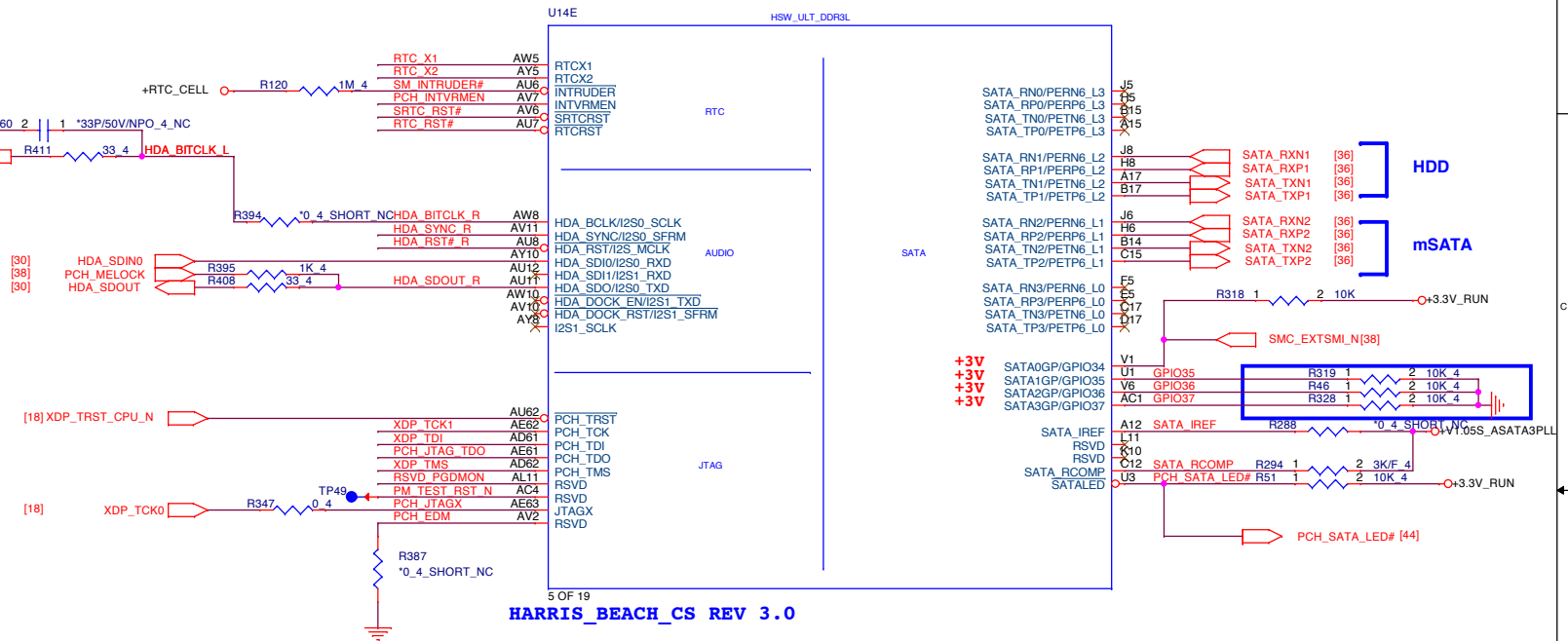


DFXTESTMODE
HIGH - DFXTESTMODE DISABLED(DEFAULT)
LOW - DFXTESTMODE ENABLED

PCH Strap Table

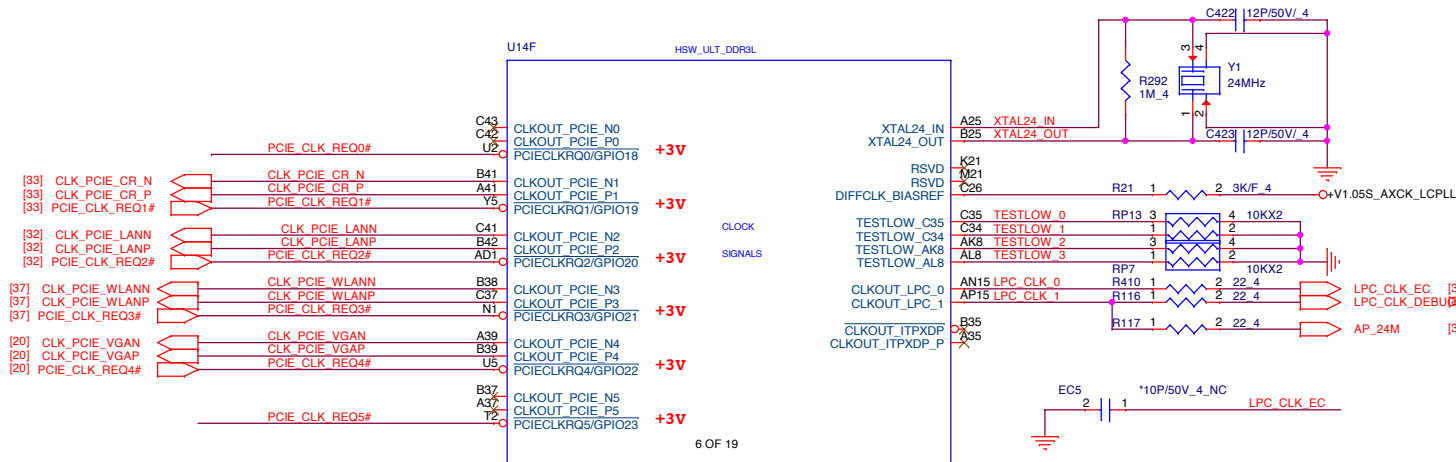
Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+RTC_CELL - R407 - *330K 4 NC PCH_INTVRMEN R392 - *330K 4

Haswell ULT (RTC, HDA, JTAG, SATA)

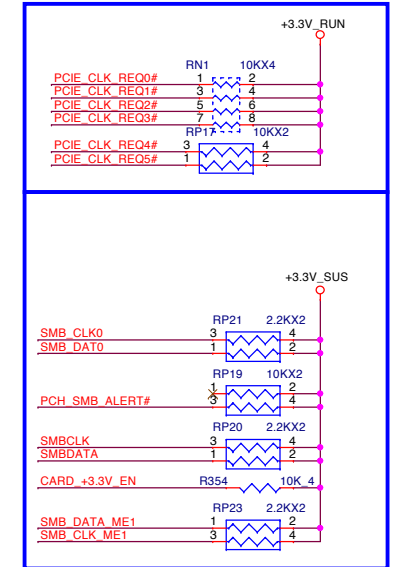
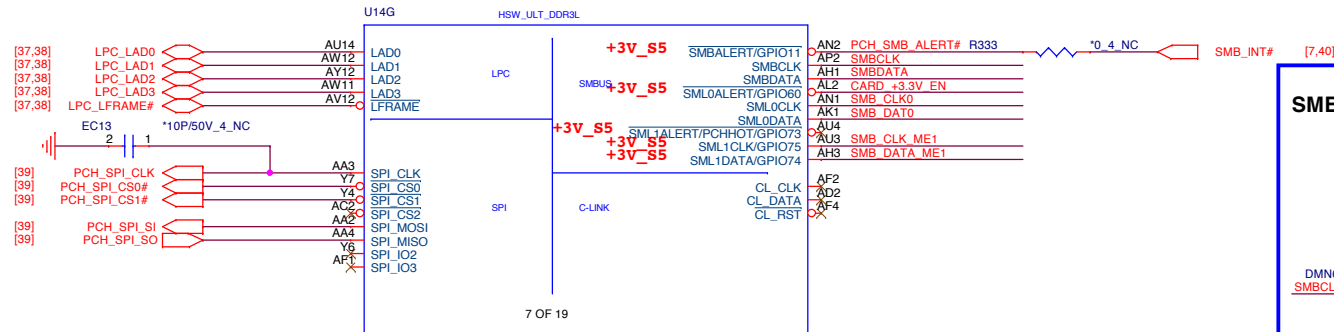


HARRIS_BEACH_CS REV 3.0

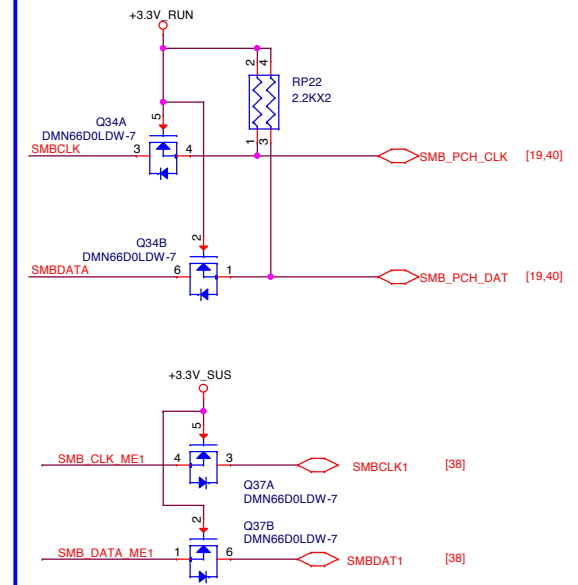
Haswell ULT (CLK)



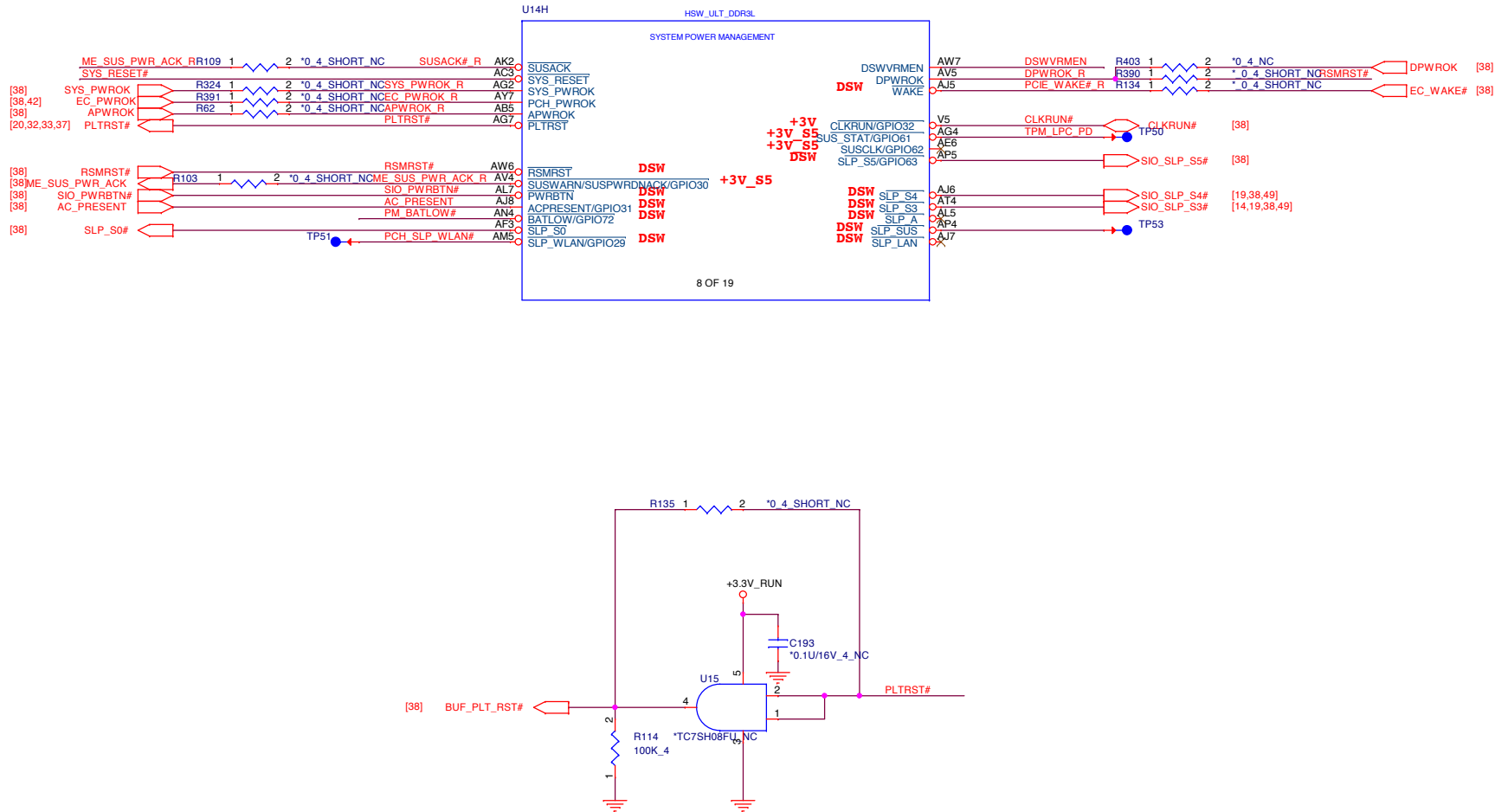
Haswell ULT (LPC/SPI/SMB/CLINK)



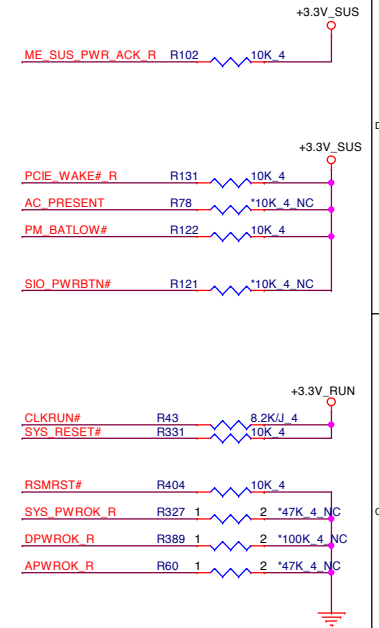
SMBus/Pull-up(CLG)



Haswell ULT (SYSTEM POWER MANAGEMENT)



PCH Pull-high/low(CLG)



+RTC_CELL

R406
330K_4

DSWVRMEN

On Die DSW VR Enable
High = Enable (Default)
Low = Disable



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PROJECT : JW8B

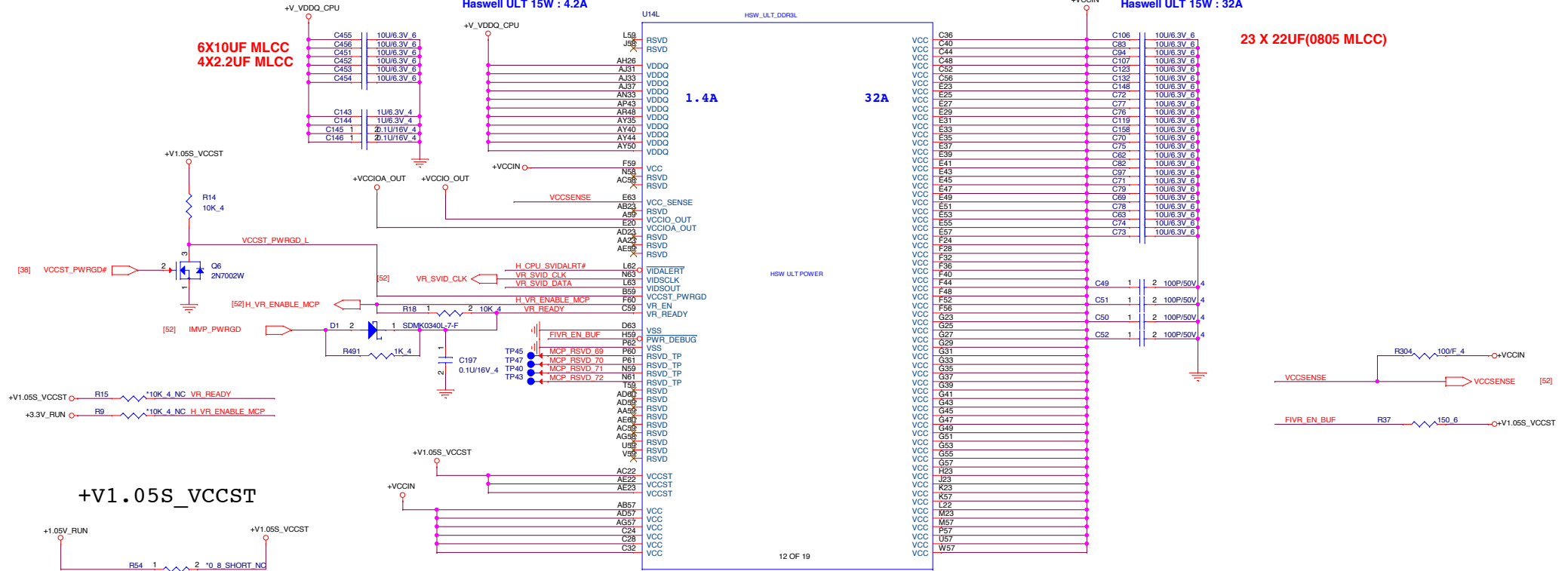
Haswell ULT MCP (POWER)

CPU VDDQ
Haswell ULT 15W : 4.2A

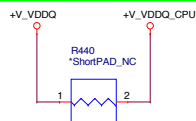
CPU VCC 1/21: 220x23 --> 100x23
Haswell ULT 15W : 32A

6X10UF MLCC
4X2.2UF MLCC

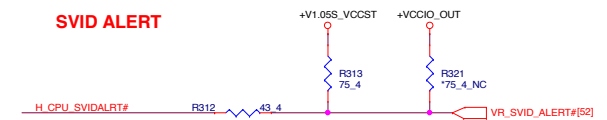
23 X 22UF(0805 MLCC)



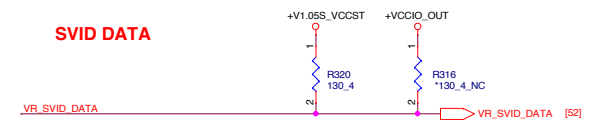
S3 Power reduce



SVID ALERT

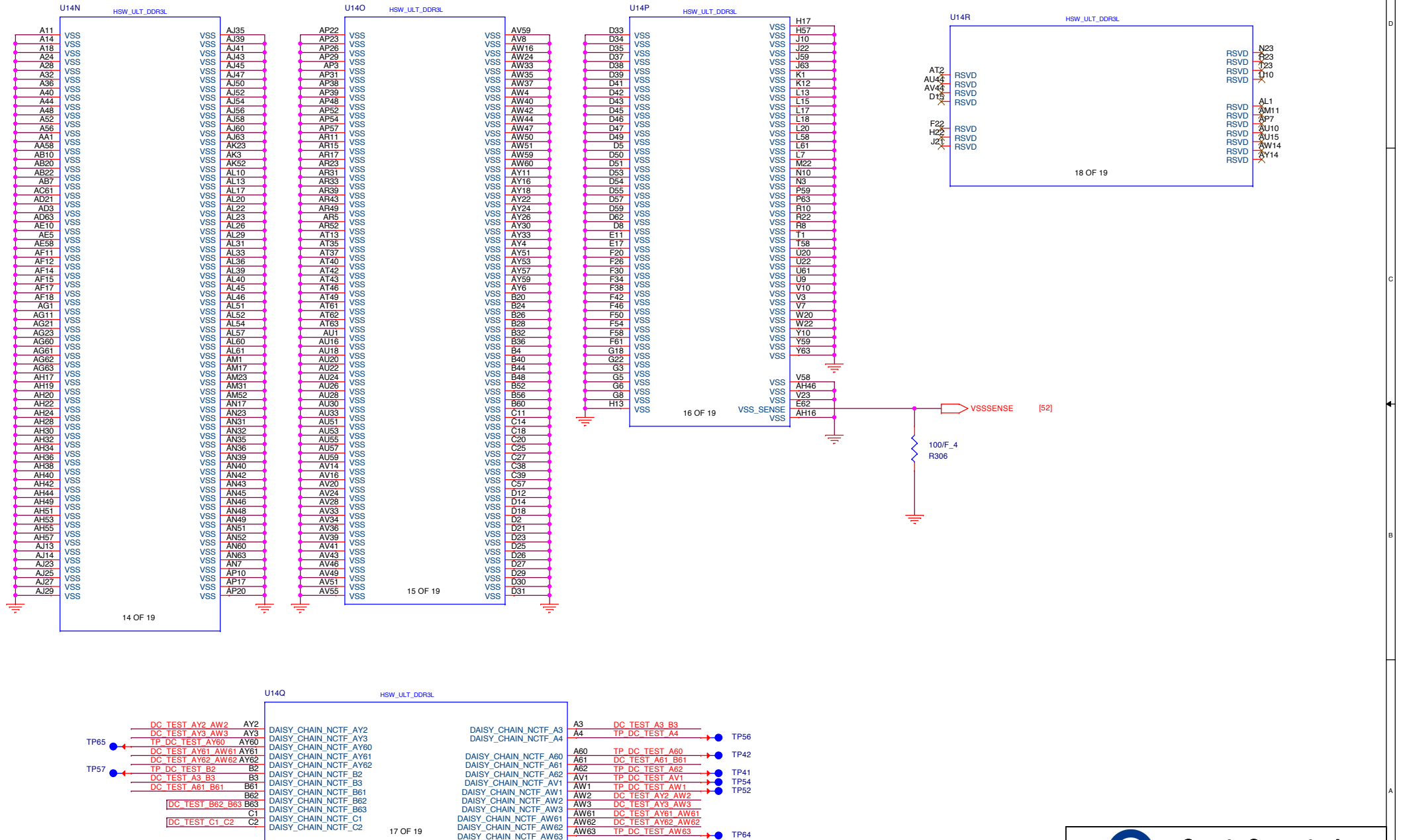


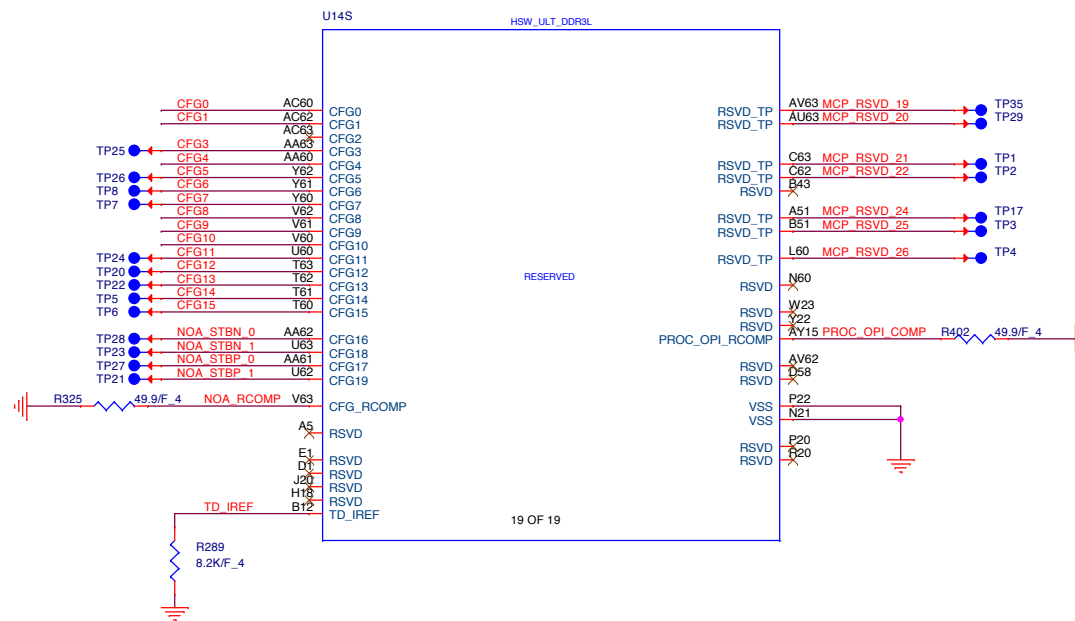
SVID DATA



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Haswell ULT (GND)





Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R339 *1K 4 NC
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R334 *1K 4 NC
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG3 R330 *1K 4 NC
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R61 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R326 *1K 4 NC
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R58 *1K 4 NC
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R57 *1K 4 NC


```

3.3 SUS: 205mA
1.05 SUS: 2066mA
1.05 RUN: 2578mA
3.3 RUN: 58mA

```

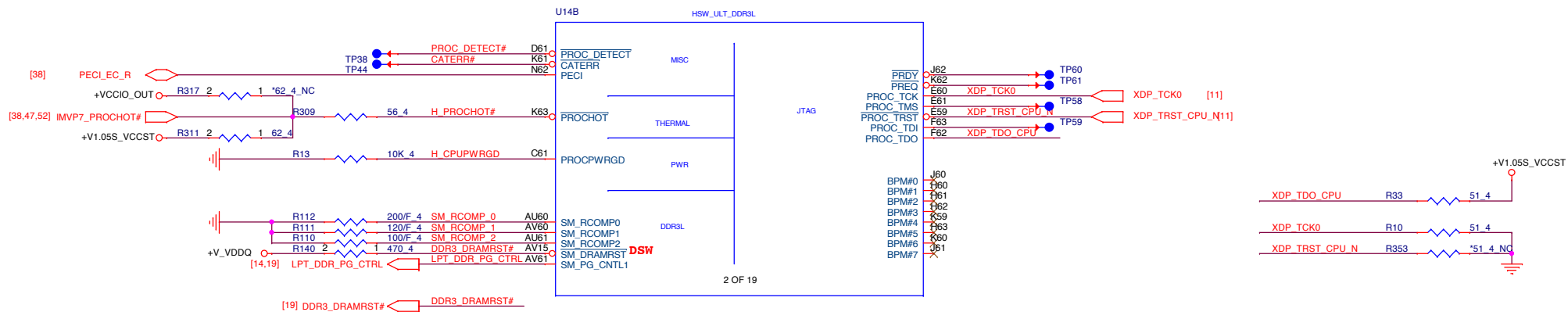


VCCSUS3
129mA

VCC1_05
2.6A

VCCASW
473mA





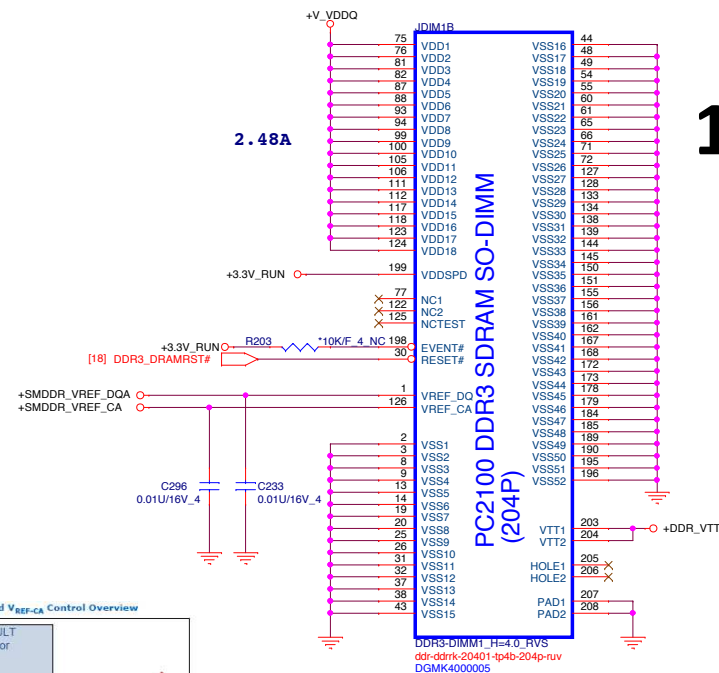
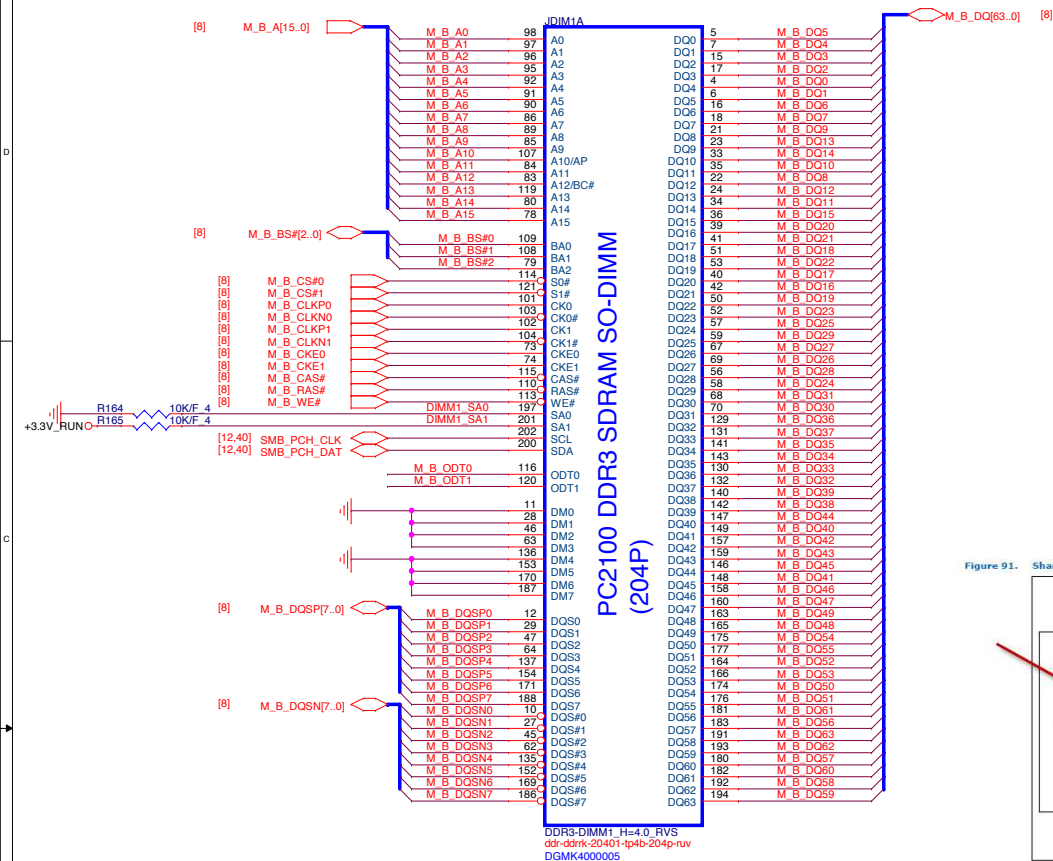
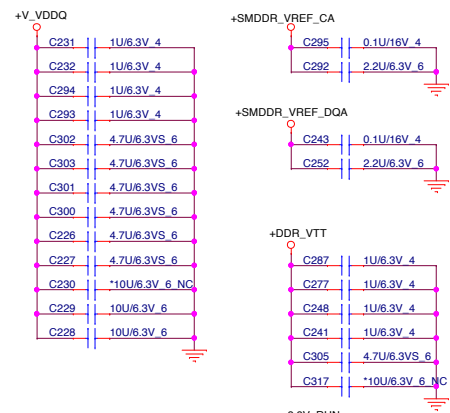
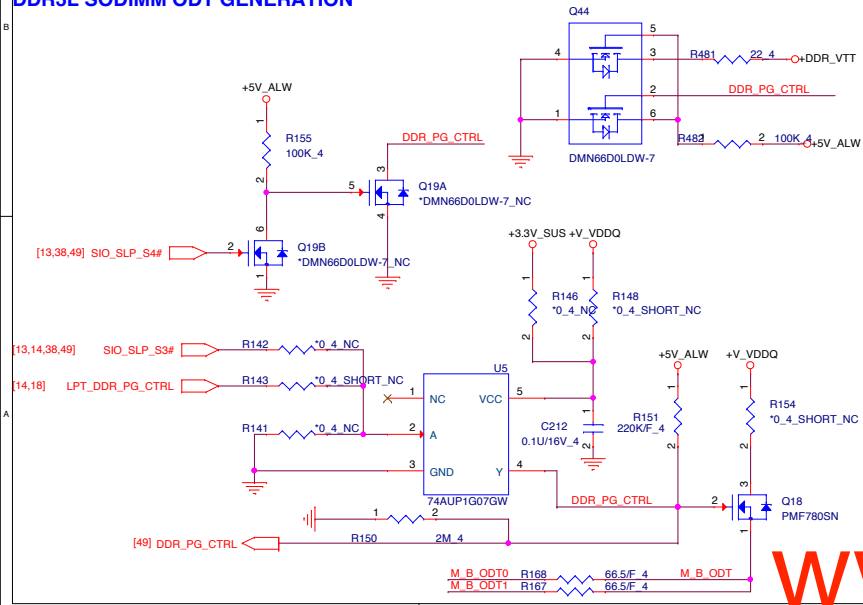
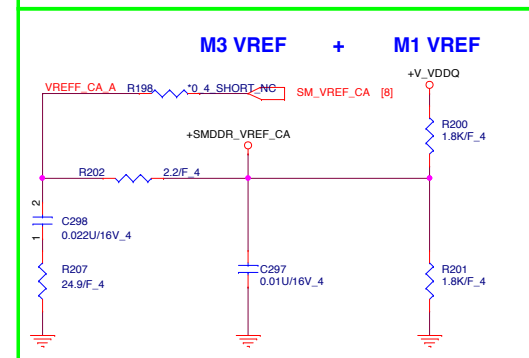
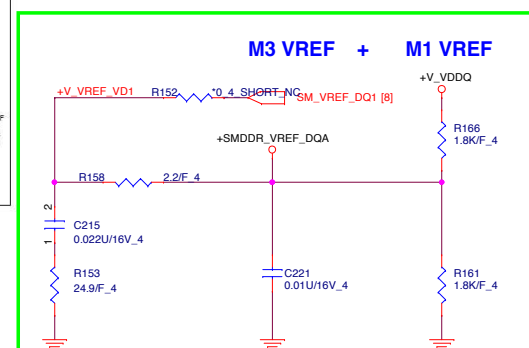
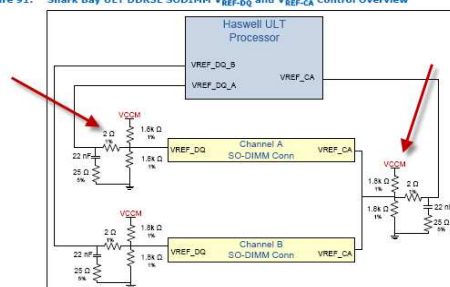
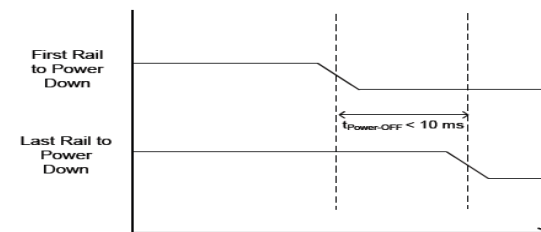
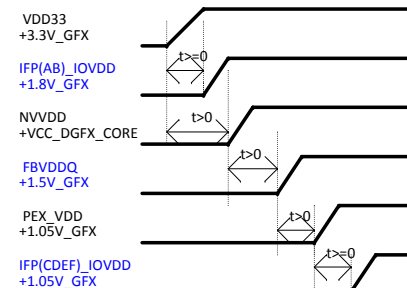
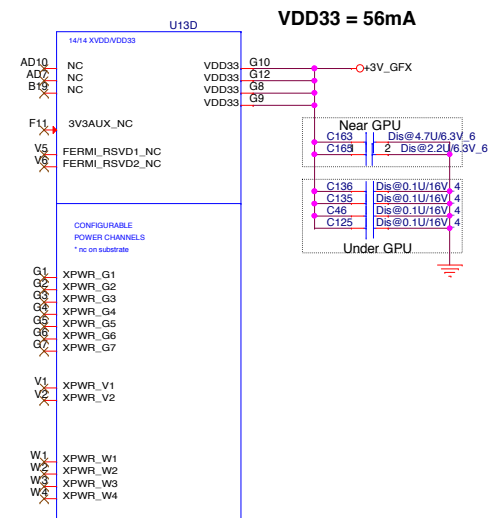
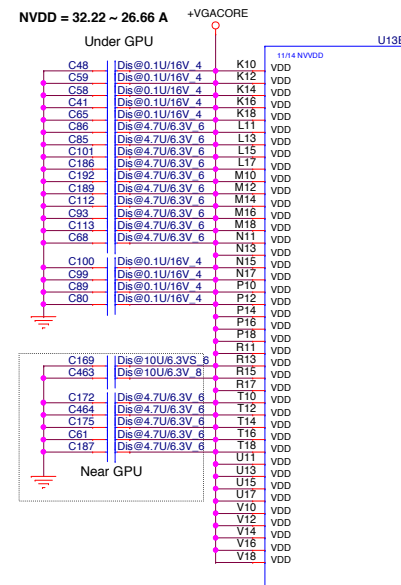
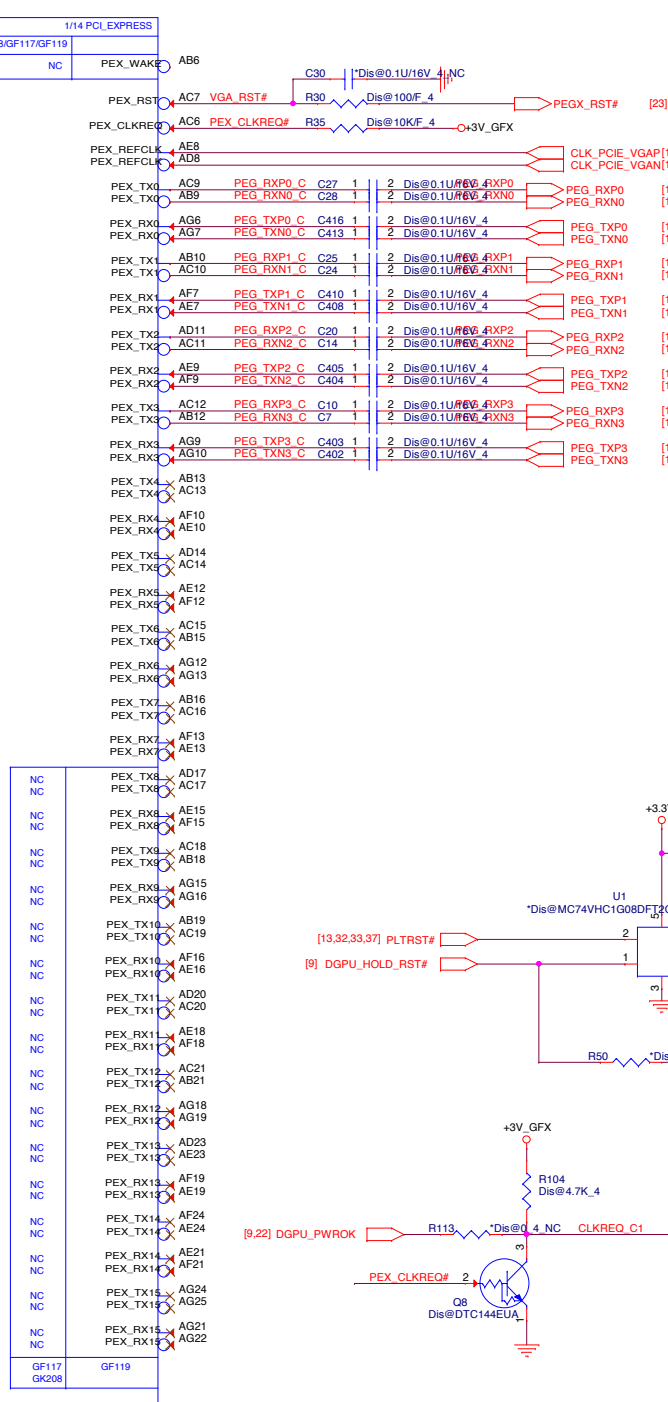
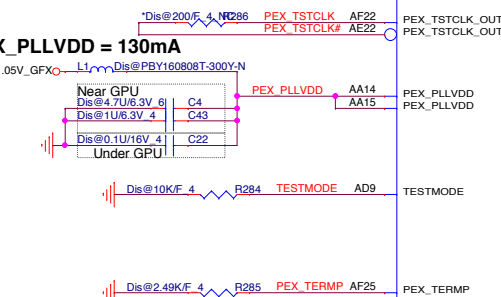


Figure 91. Shark Bay ULT DDR3L SODIMM V_{REF-DQ} and V_{REF-CA} Control Overview

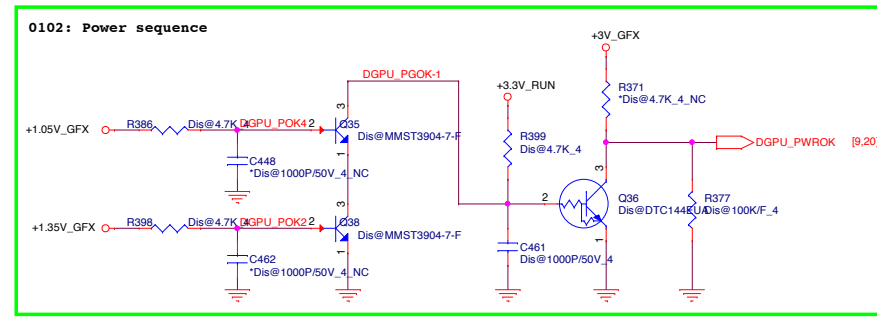
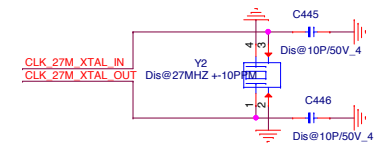
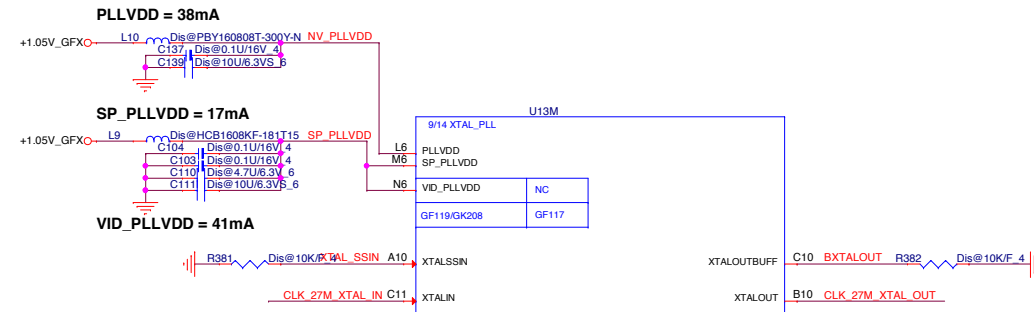
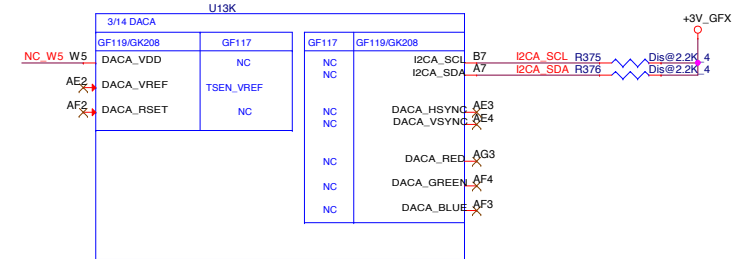
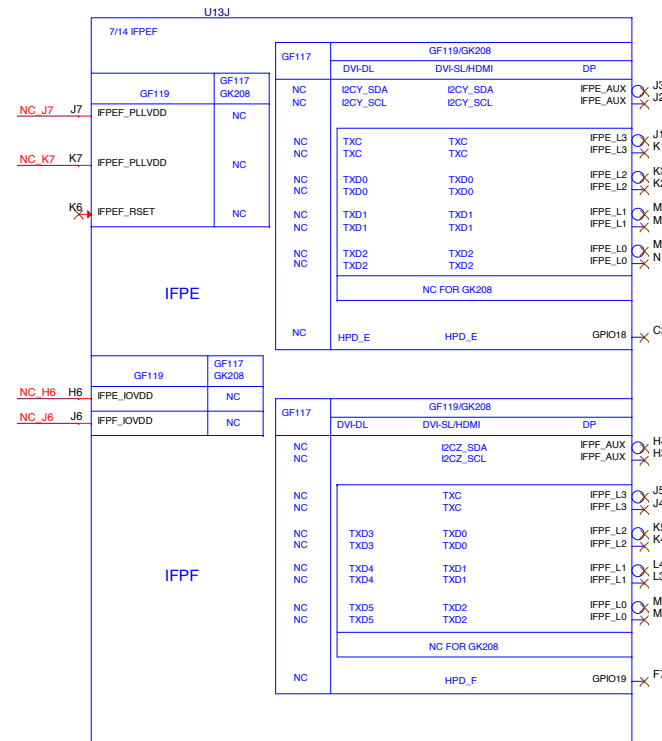
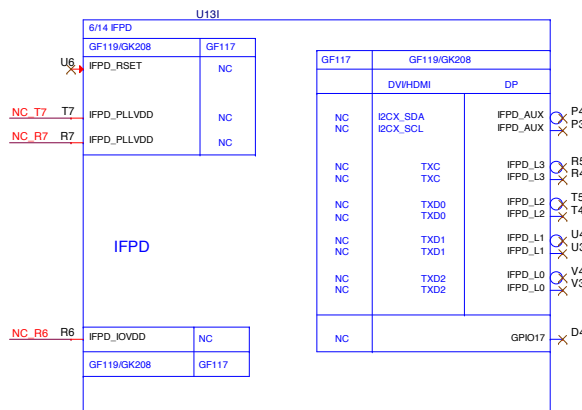
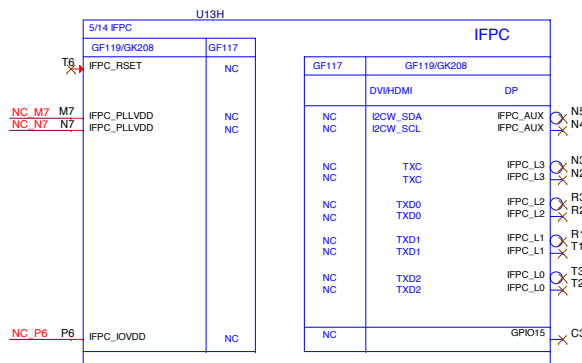
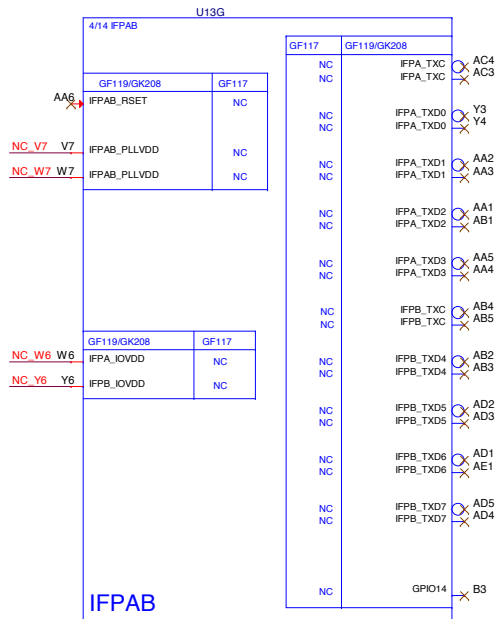


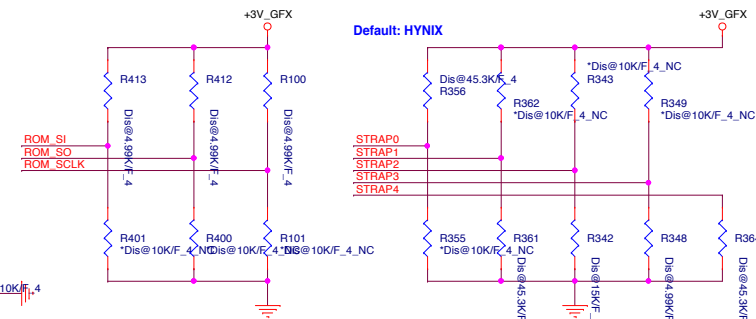
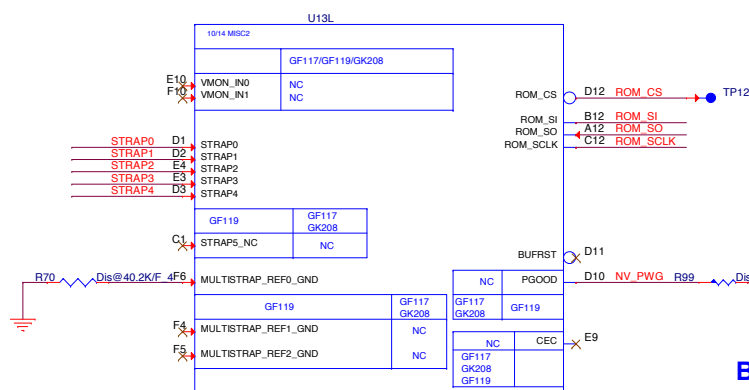
PEX IOVDD + PEX IOVDDQ = 1.042A

**PEX_PLL_HVDD +
PEX_SVDD 3V3 = 143mA**









4.99K: CS24992FB00 RES CHIP 4.99K 1/16W +1% (0402)
 45K: CS34502FB00 RES CHIP 45K 1/16W +1% (0402)
 15K: CS31502FB24 RES CHIP 15K 1/16W +1% (0402)
 30.1K: CS33012FB18 RES CHIP 30.1K 1/16W +1% (0402)
 34.8K: CS33482FB22 RES CHIP 34.8K 1/16W +1% (0402)

Binary Strap Mode Mapping

Strap Pin name	Strap Mapping	Resistance	Note
ROM_SCLK	PCI_DEVID[4] SUB_VENOR PCI_DEVID[5] PEX_PLL_EN	5Kohm , H	1000 , SUB: no Video BIOS
ROM_SI	RAM_CFG[2] RAM_CFG[1] RAM_CFG[0]	5Kohm , H	4.99K 1000 --> Micron MT41K128M16JT-107G:K (Default) 30.1K 1101 --> Micron MT41K256M16HA-107G:E 34.8K 1110 --> Hynix H5TC4G63AFR-11C
ROM_SO	FB[1] FB[0] SMB_ALT_ADDR VGA_DEVICE	5Kohm , H	1000 , FB: 256 MB (Default) SMB:0x9E
STRAP0	User strap [3:0]	45Kohm , H	1111 , EDID is used
STRAP1	3GIO_CFG[3:0]	45Kohm , D	1111 , USER defined
STRAP2	PCI_DEVID[3:0]	15Kohm , D	010010 , N14P-GV2
STRAP3	SOR[3:0]_EXPOSED	5Kohm , D	0000 , IFPx port not use
STRAP4	RESERVED PCIE_SPEED_GEN3 PCIE_MAX_SPEED DP_PLL_VDD33V	45Kohm , D	0111 , PCIE GEN3 setting

GPIO ASSIGNMENTS (GB2-64)

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	MEMORY VDD ID
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5		RESERVE	
6	OUT	FB_CLAMP_TGL_REQ#	# --> FB Clamp toggle request
7	OUT	3DVision	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM_VREF_CTL	MEMORY VREF CONTROL
11	OUT	PWM_VID	GPU Core VDD PWM control
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	PSI	Phase Shedding
14	IN	HPD_A	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	FRM_LCK	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F or HPD_B	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

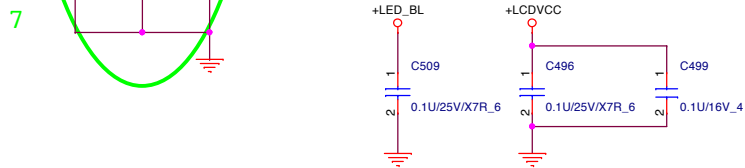
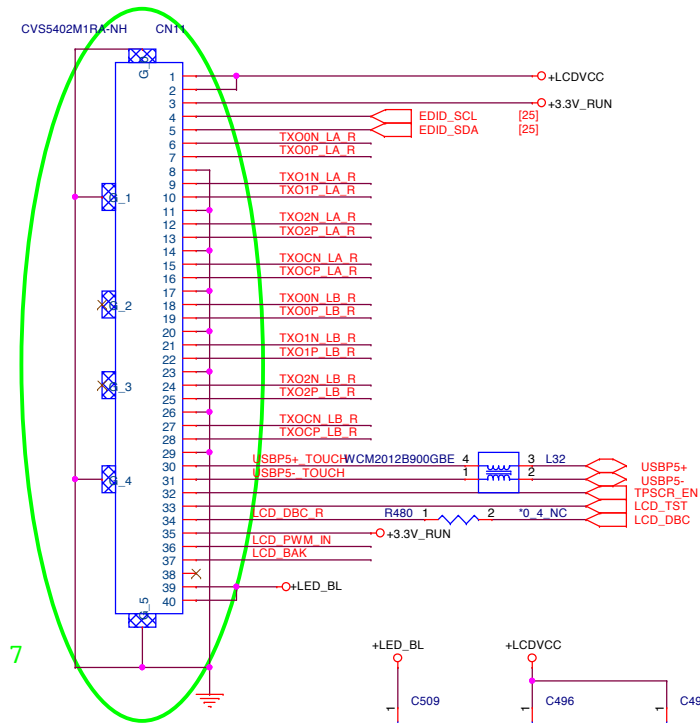
VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	DELL P/N	QC1 P/N
0000				
1000 0x8	MT41K128M16JT-107G:K (FCBGA)(96P)	Micron	NA	AKD5DGSTL00
1101 0xD	MT41K256M16HA-107G:E	Micron	NA	AKD5PGSTL00
1110 0xE	H5TC4G63AFR-11C	Hynix	NA	AKD5PGWTW05

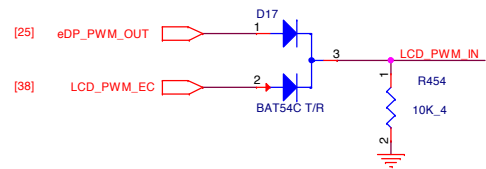
for meet Power down sequence for +3V_GFX

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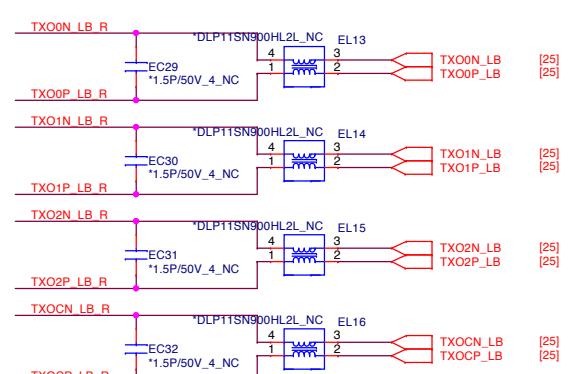
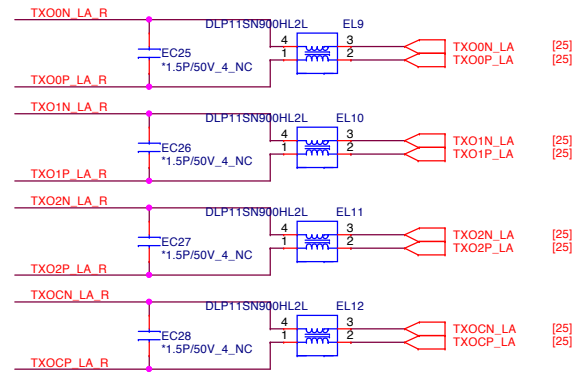
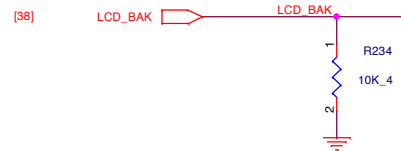




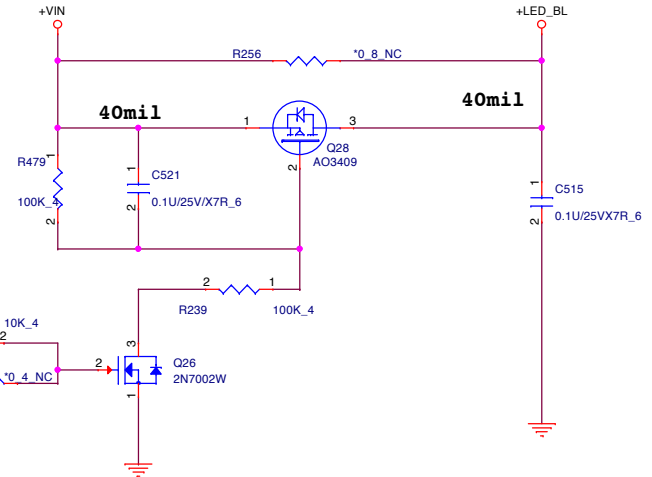
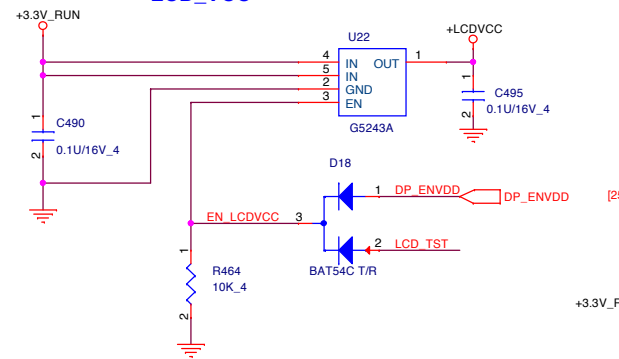
Brightness Control

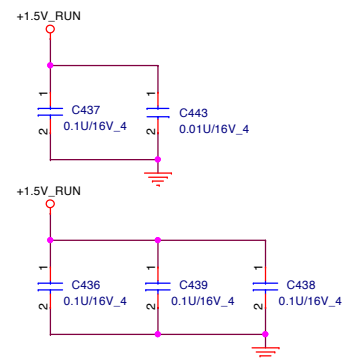


BAK_EN

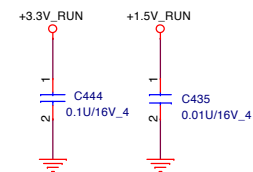


LCD_VCC

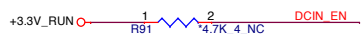




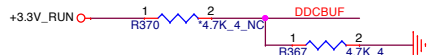
[7] INT_HDMI_TXP2
[7] INT_HDMI_TXN2
[7] INT_HDMI_HP
[7] INT_HDMI_TXP1
[7] INT_HDMI_TXN1
[7] INT_HDMI_TXP0
[7] INT_HDMI_TXN0
[7] INT_HDMI_TXCP
[7] INT_HDMI_TXCN



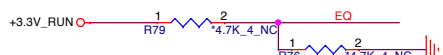
3 Level Input:
L:LOW,internal pull down
H:HIGH, external pull up
M:VDD3/2, both external pill-up and pull-down



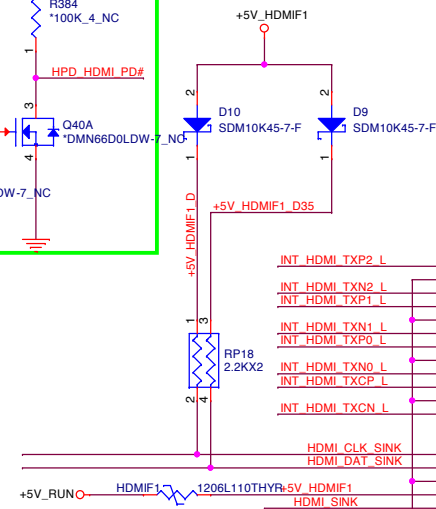
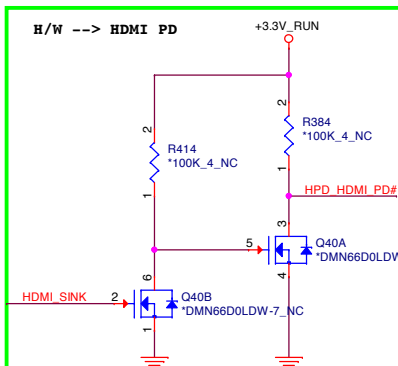
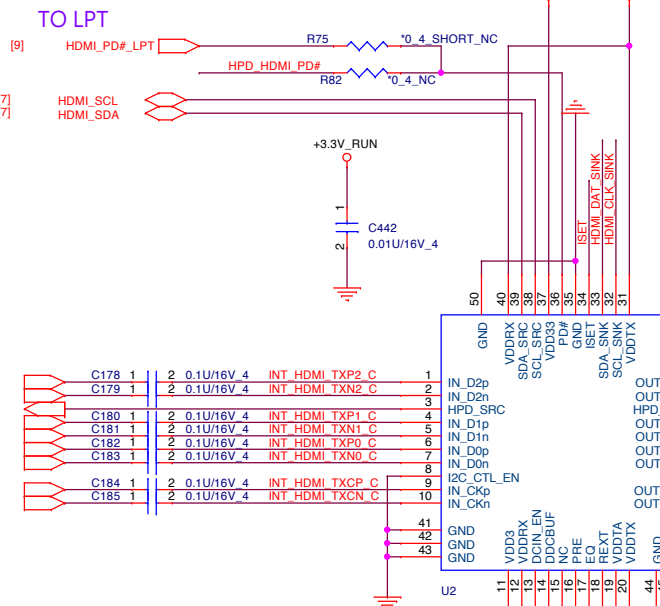
Int pull-down 150k , 3.3V IO
L:default,AC coupling input
H:DC coupling input



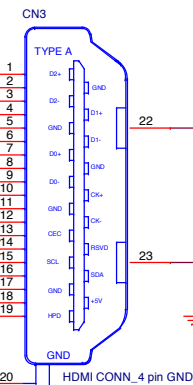
L:default,passive DDC pass-through
H:active DDC buffer with default threshold
M:passive DDC pass-through with internal -10Kohm pull up



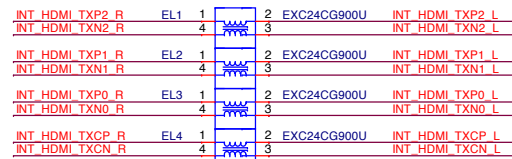
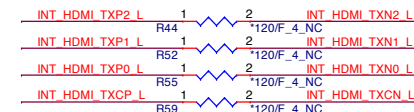
L:programmable EQ for channel loss up to 6.5dB @3Gbps
H:programmable EQ for channel loss up to 9.5dB @3Gbps
M:programmable EQ for channel loss up to 3dB @3Gbps



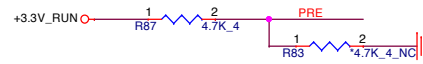
HDMI CN



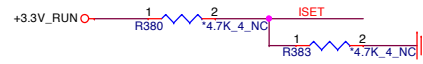
EMI



Int pull-down 150k , 3.3V IO
L:HDMI ID disable
H:HDMI ID enable



L:no pre-emphasis
H:1.6dB pre-emphasis
M:3.0dB pre-emphasis



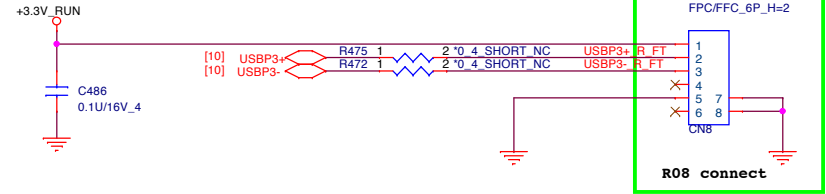
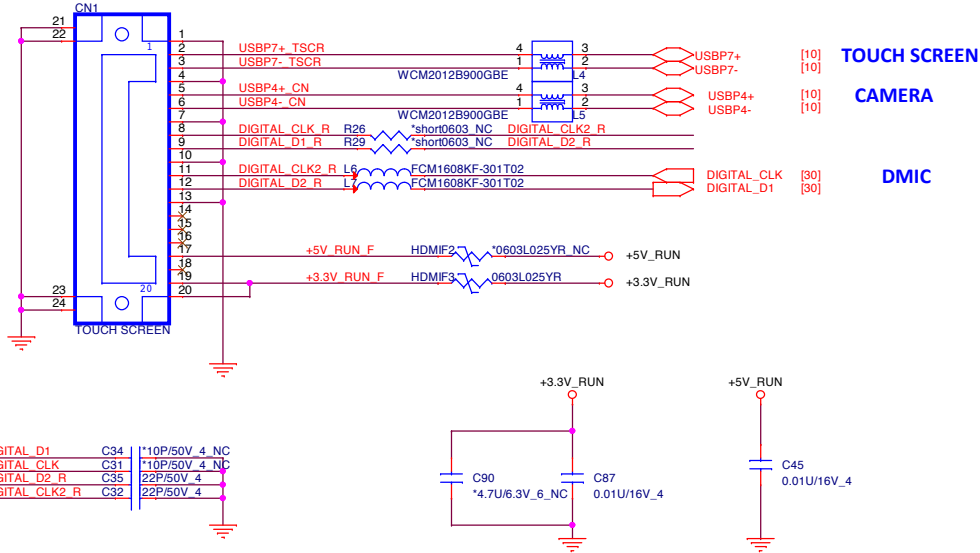
L:default
H:increase +13%
M:increase -13%

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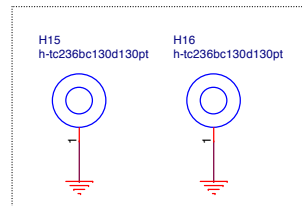
CAMERA / DMIC

Fingerprint

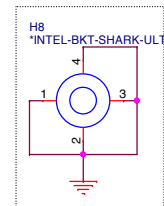
Conn P/N, Footprint OK. Luke 12/18



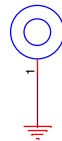
Mini-PCIE



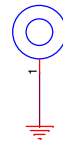
CPU BKT



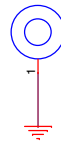
H7
*H-TC394BC315D130P2



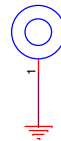
H10
*h-tc394bc315d138p2



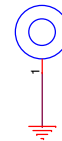
H11
*h-tc394bc315d138p2



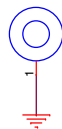
H13
*h-tc394bc315d138p2



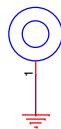
H14
*h-tc276bc315d118p2



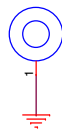
H3
*h-tc236bc315d98p2



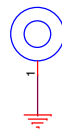
H4
*h-tc236bc315d98p2



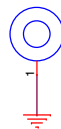
H6
*H-TSBC315D98P2



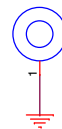
H12
*h-tc236bc315d98p2



H5
*h-tc315bc150d150pt



H9
*h-tc315i190bc150d150pt

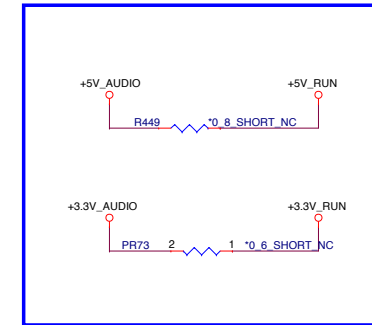
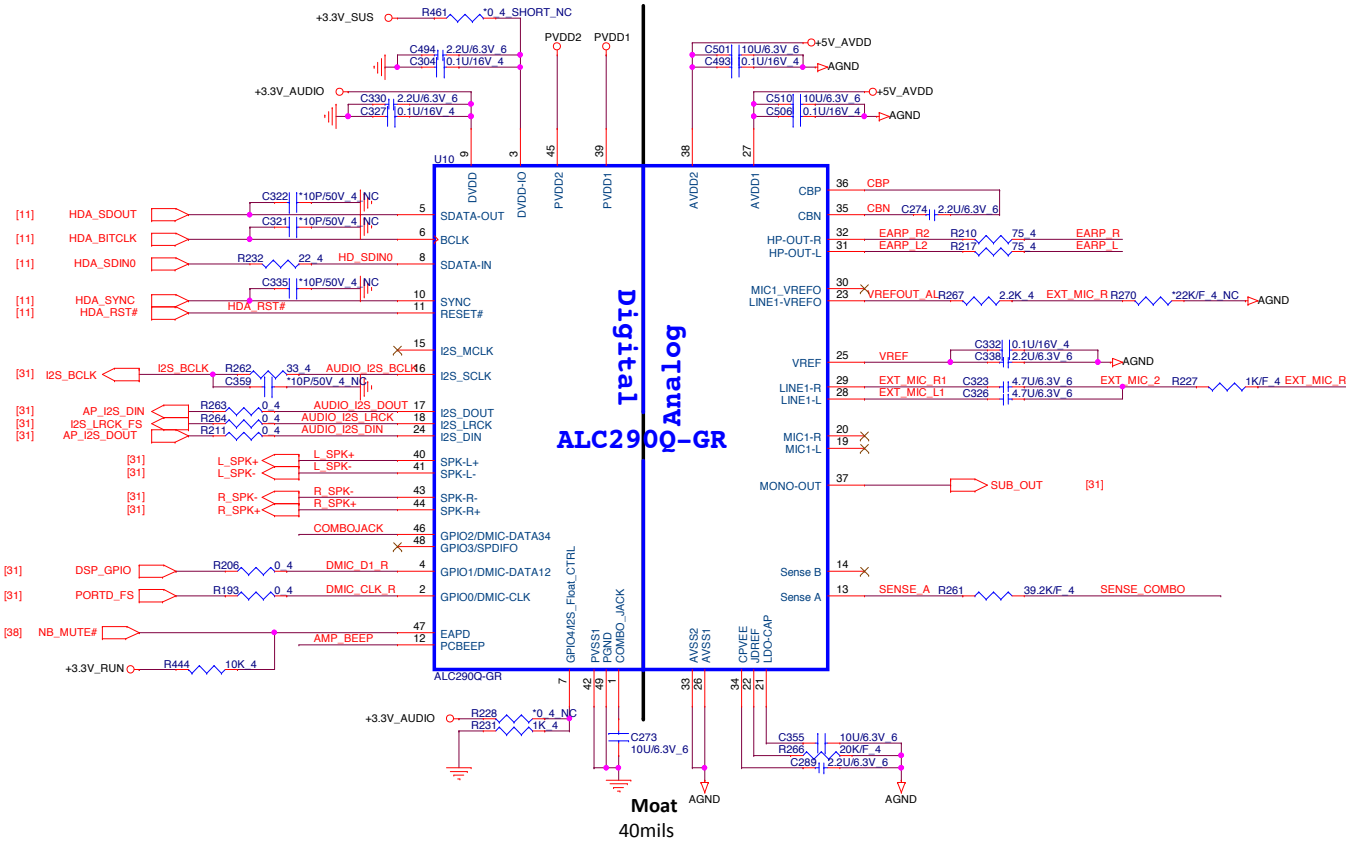
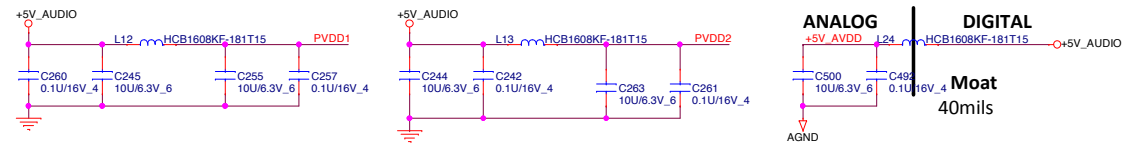


H1
*h-c59d59n

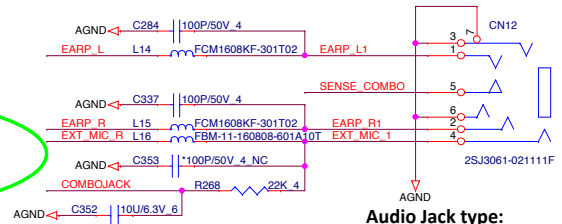


H2
*h-c59d59n

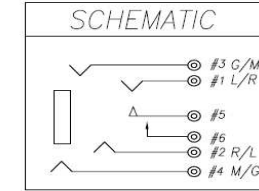
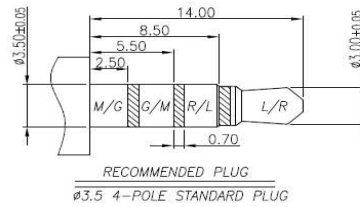
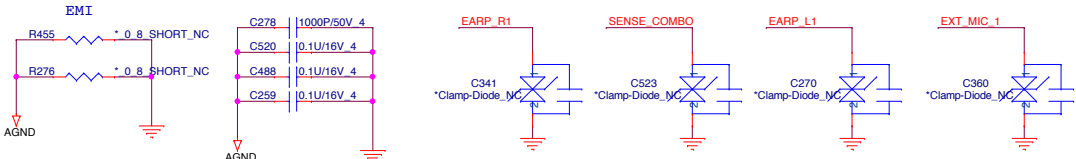
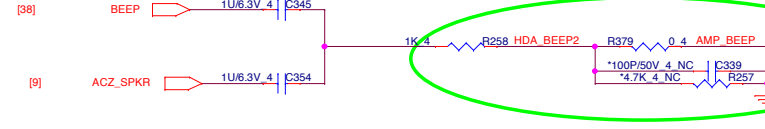
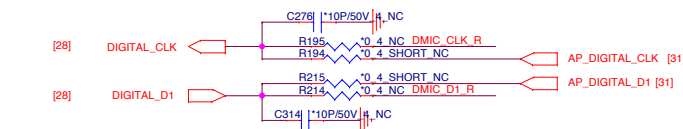




Audio Combo Jack

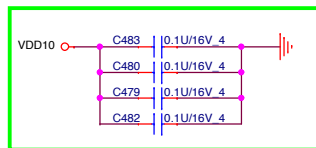


Audio Jack type:
Normal Open
Combo Jack(IPHONE)

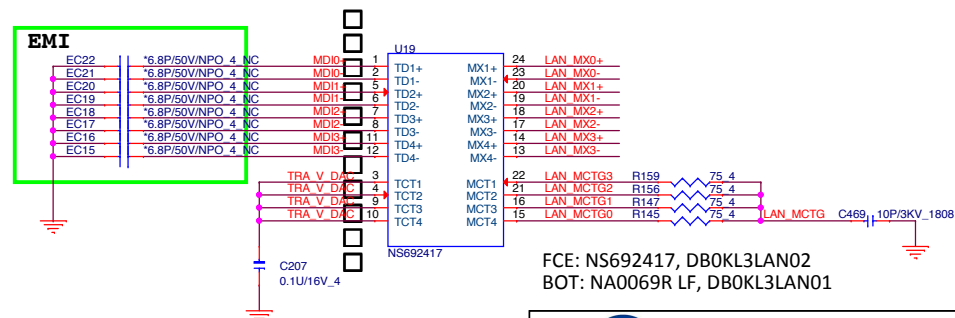
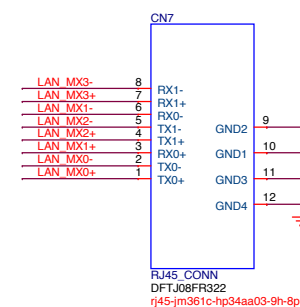
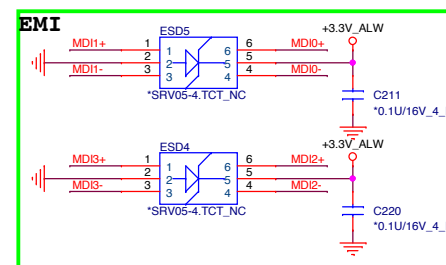
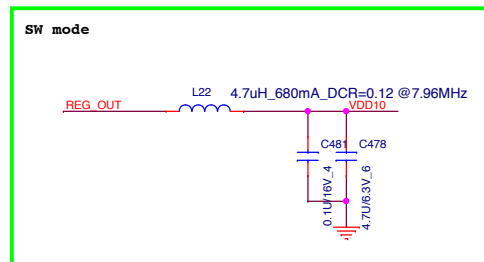
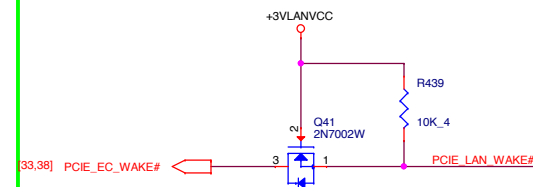
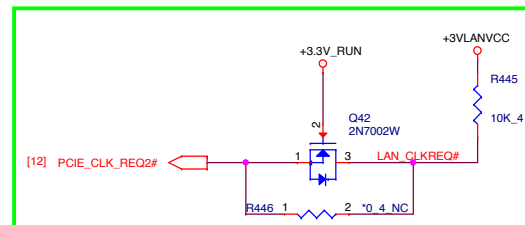
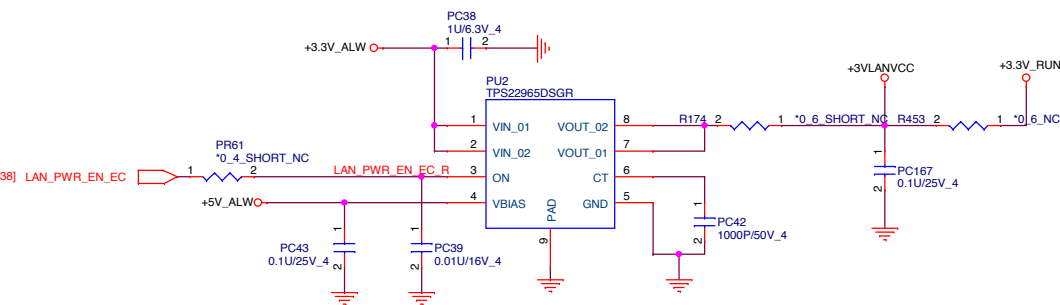
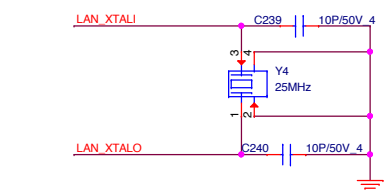
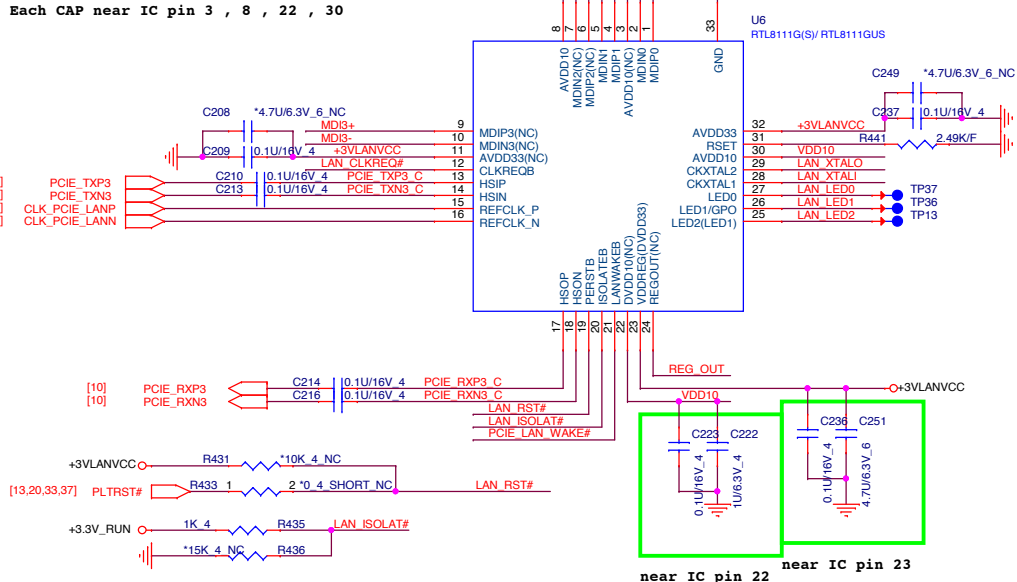


Quanta Computer Inc. PROJECT : JW8B	
Size	Document Number
Audio Codec ALC290	
Date: Wednesday, July 17, 2013	Sheet 30 of 57

JW8 have support S5 wave up

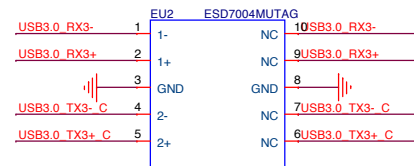
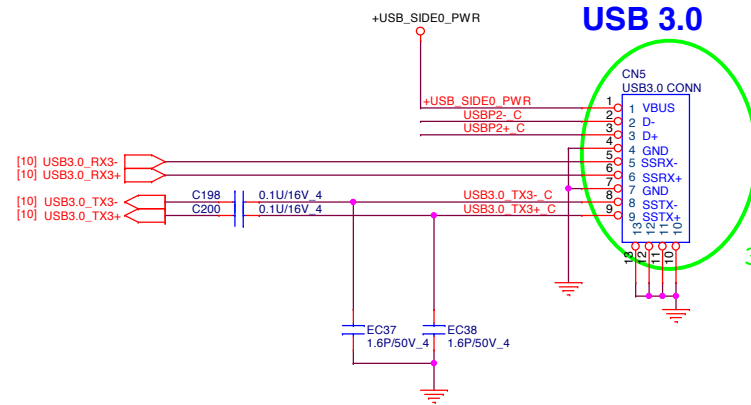
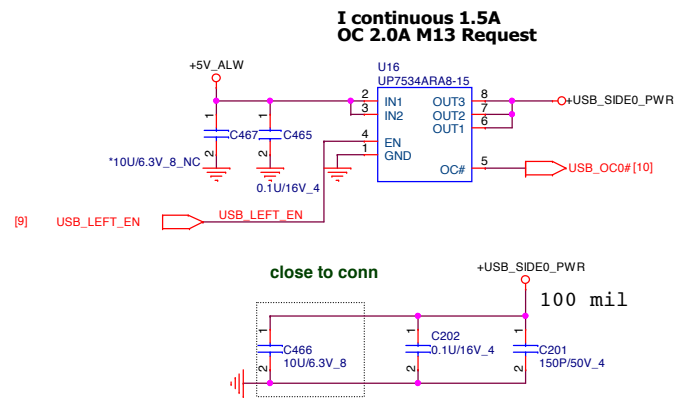


Each CAP near IC pin 3, 8, 22, 30

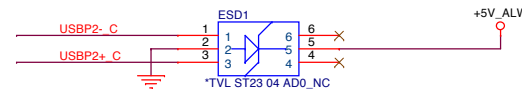


FCE: NS692417, DBOKL3LAN02
BOT: NA0069R LF, DBOKL3LAN01

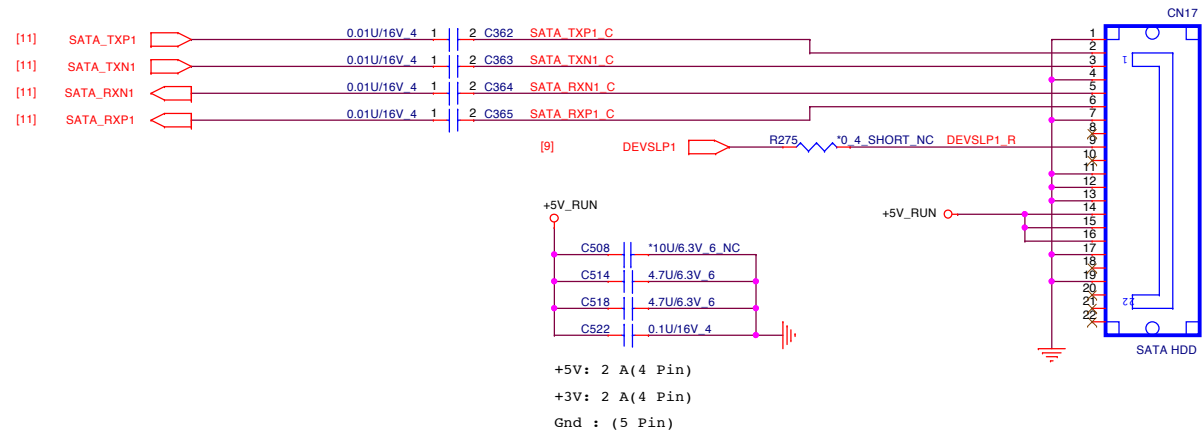
USB 3.0



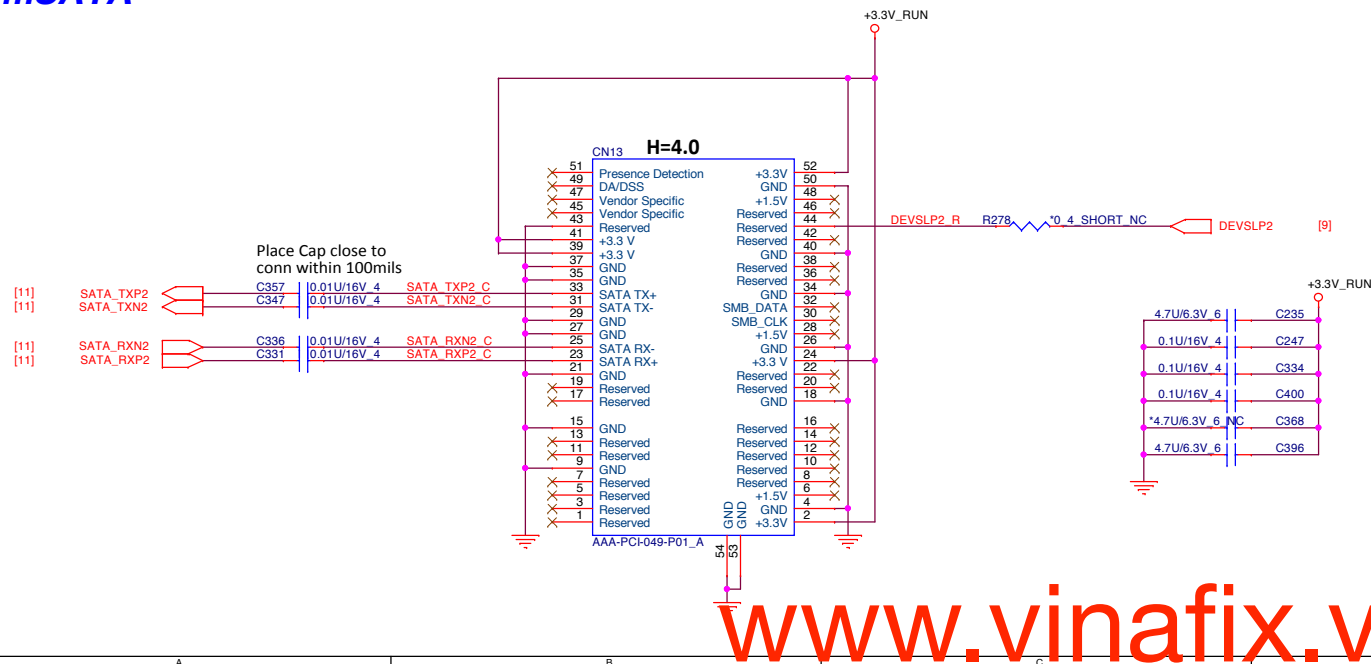
ESD Function
Place ESD diodes as close as USB connector.



SATA HDD Connector

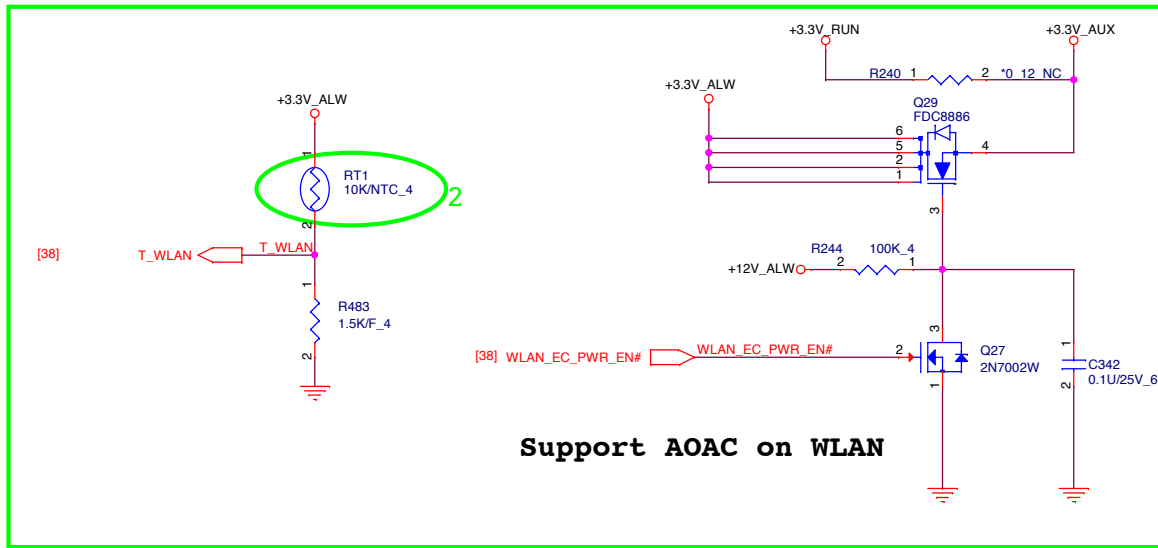
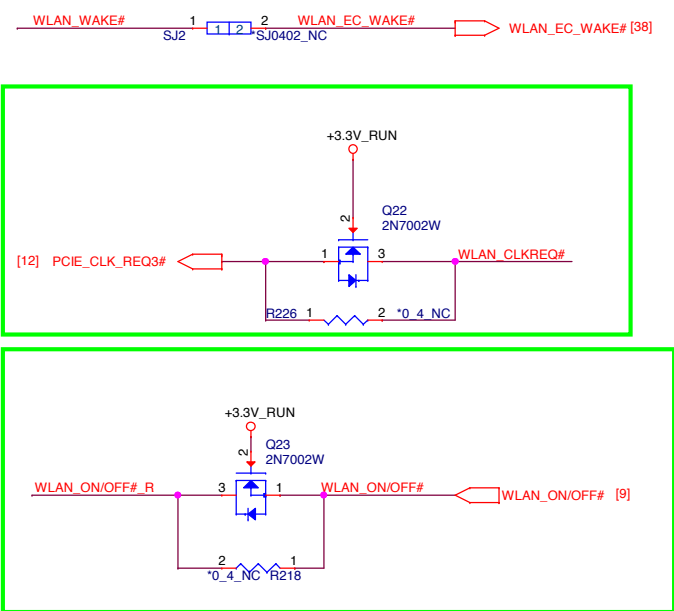
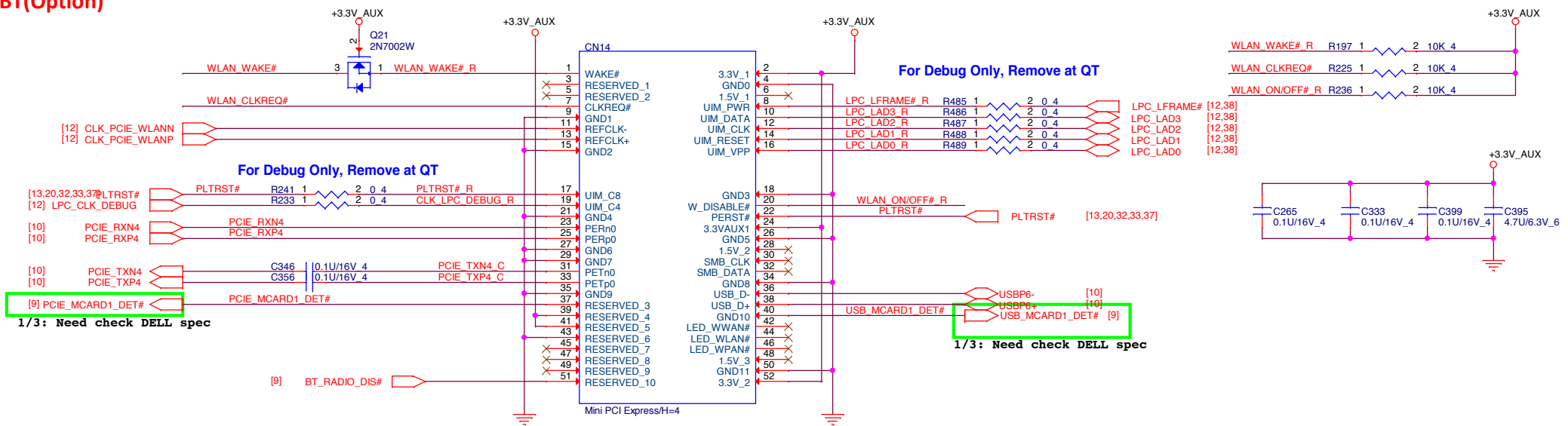



mSATA



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Mini Card
WLAN/BT(Optional)



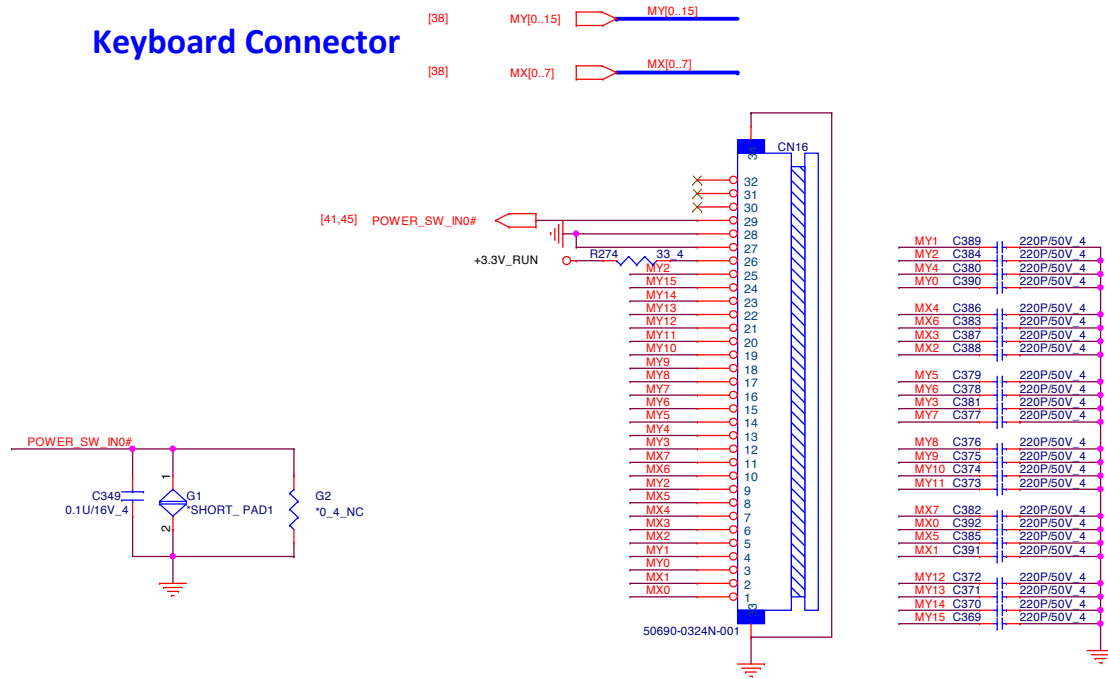


Quanta Computer Inc.
PROJECT : JW8B

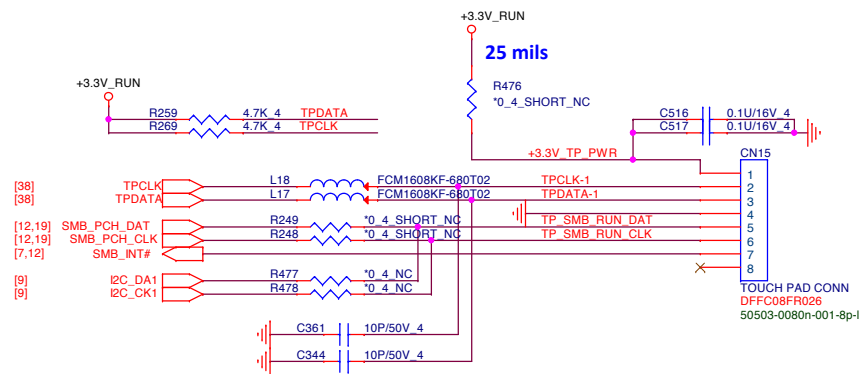
Size	Document Number	Rev
	WLAN/BT	A
Date:	Monday, July 08, 2013	Sheet 37 of 57



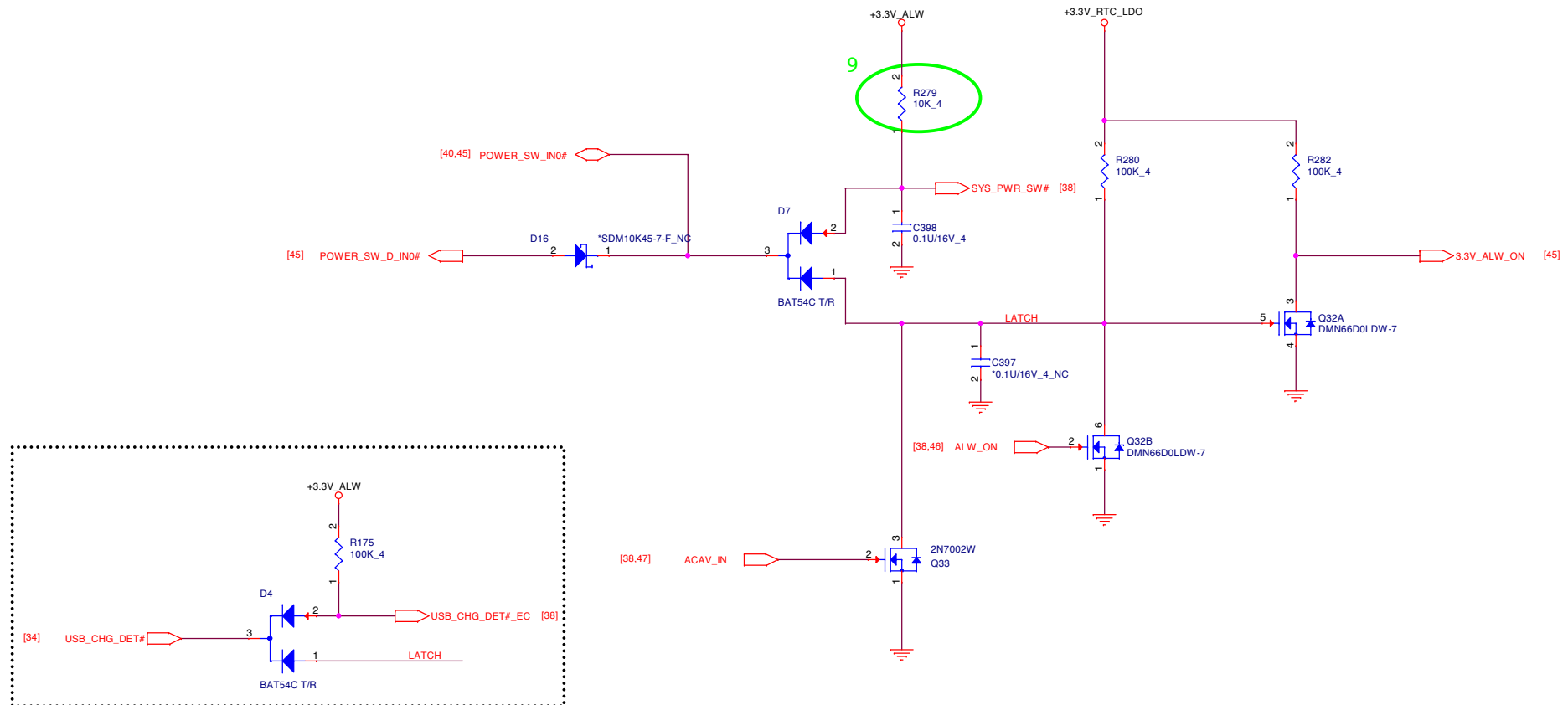
Keyboard Connector



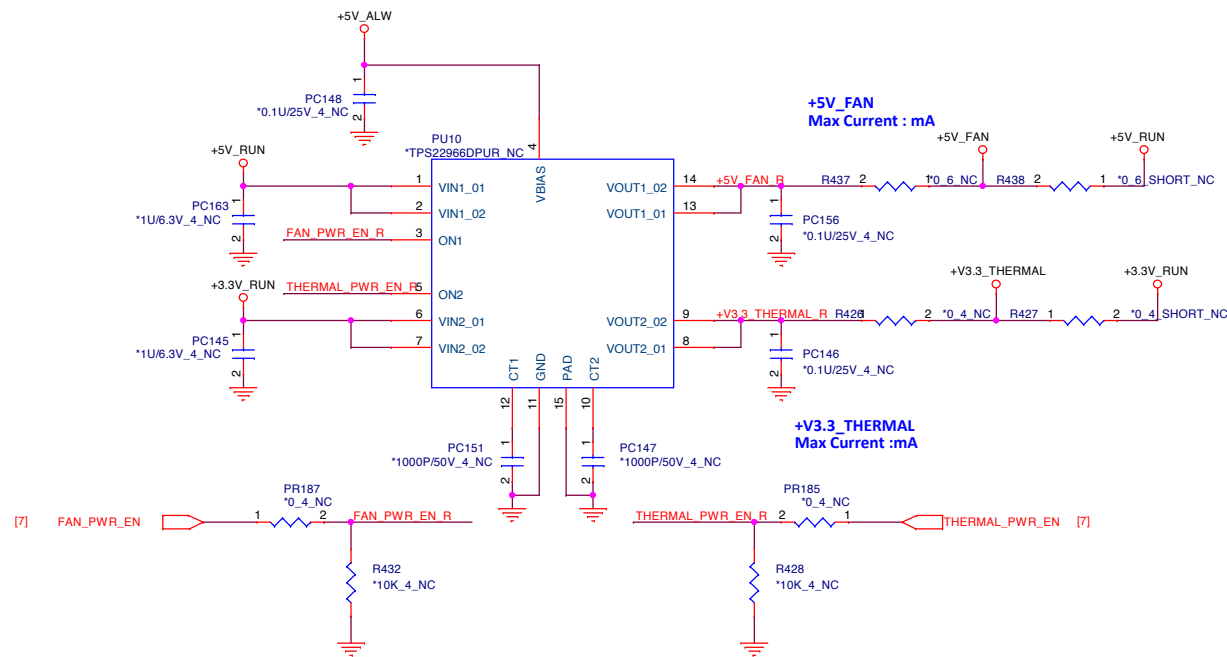
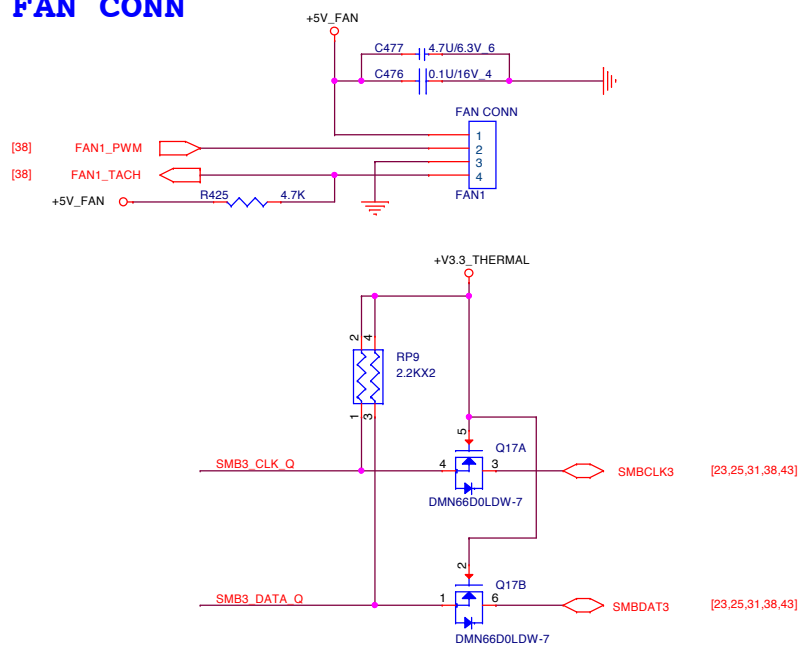
Touch Pad Connector



3VALW ON POWER LOGIC

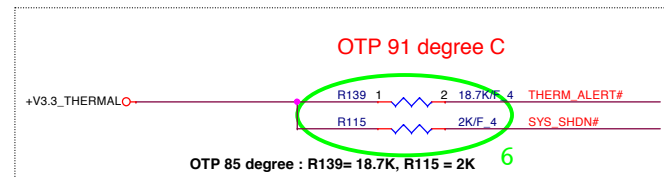
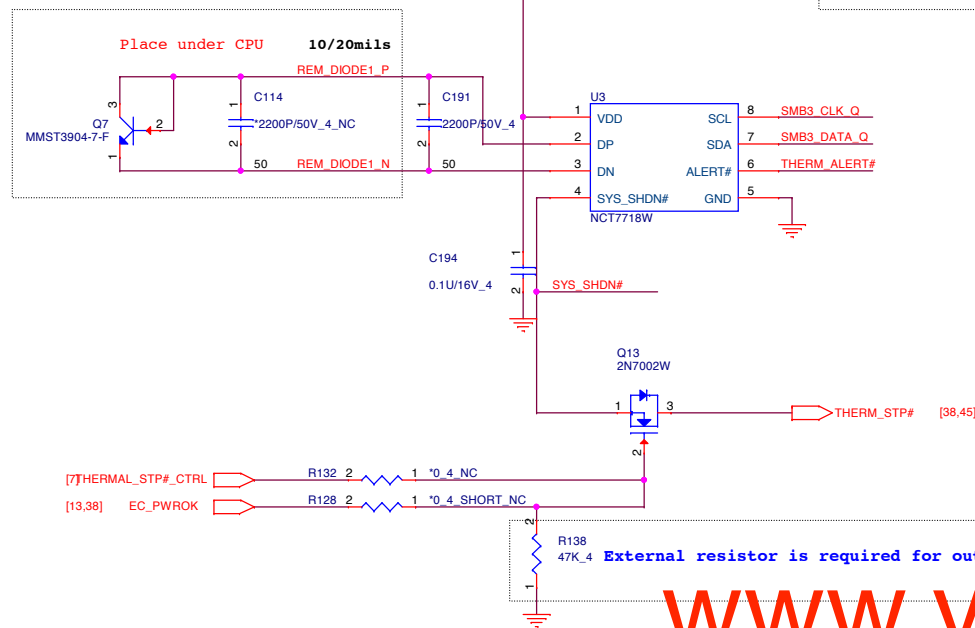


FAN CONN



THERMAL IC

Need closed to CPU

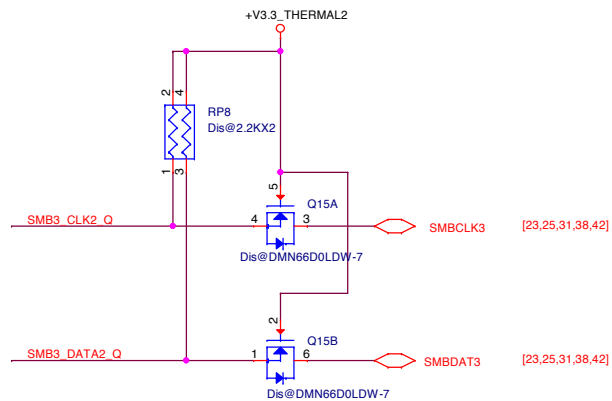
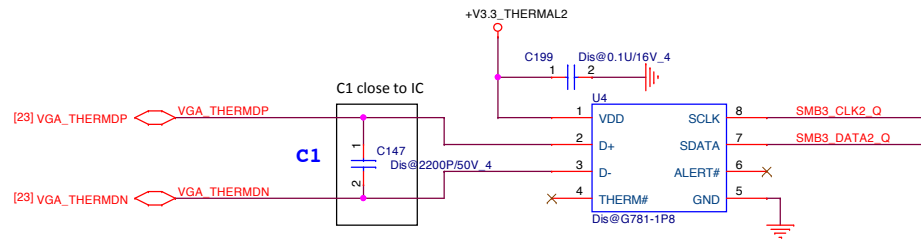


SYS_SHD#	2K	7.5K	10.5K	14K	18.7K
ALERT#					
2K	77 'C	87 'C	97 'C	107 'C	117 'C
7.5K	79 'C	89 'C	99 'C	109 'C	119 'C
10.5K	81 'C	91 'C	101 'C	111 'C	121 'C
14K	83 'C	93 'C	103 'C	113 'C	123 'C
18.7K	85 'C	95 'C	105 'C	115 'C	125 'C

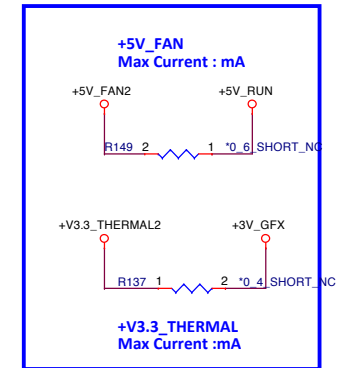
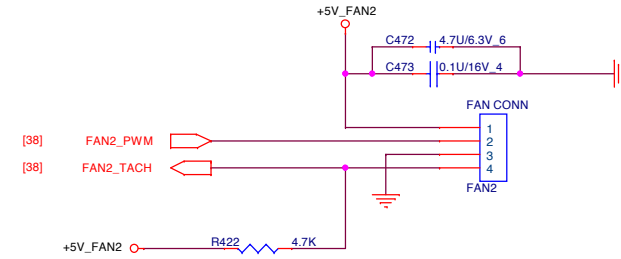
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For GPU use

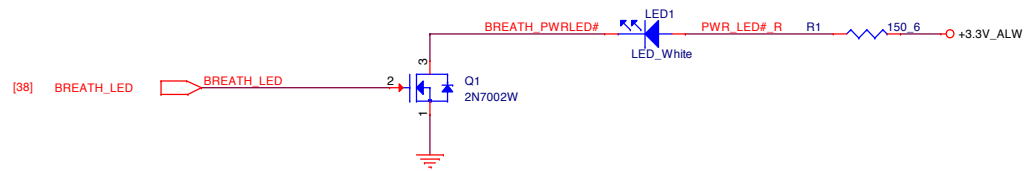
G781-1P8
SMBus address is 1001101xb (9Ah) (x is R/W bit).



FAN CONN

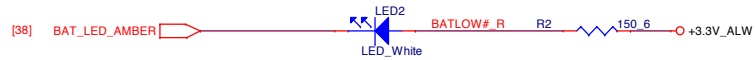


LED Status

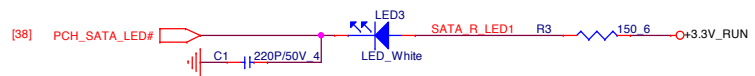


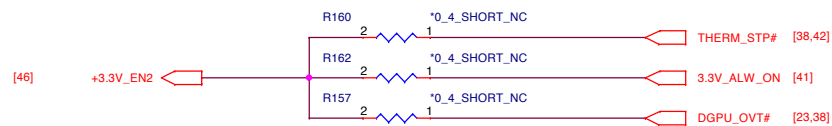
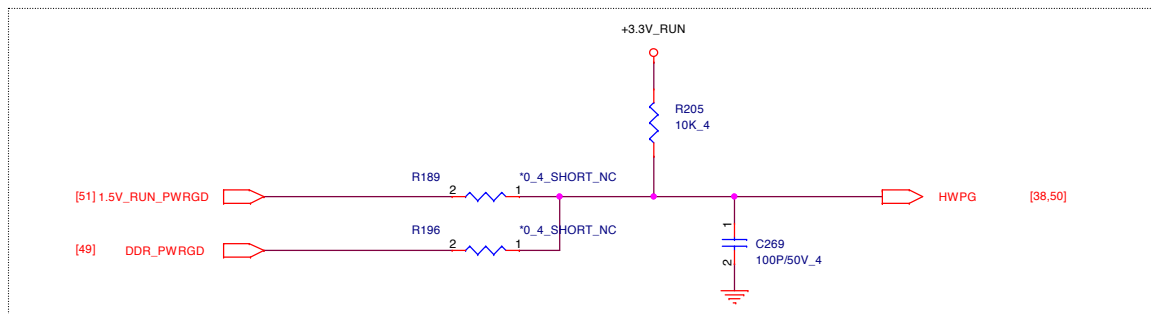
System status LED

Battery charger LED

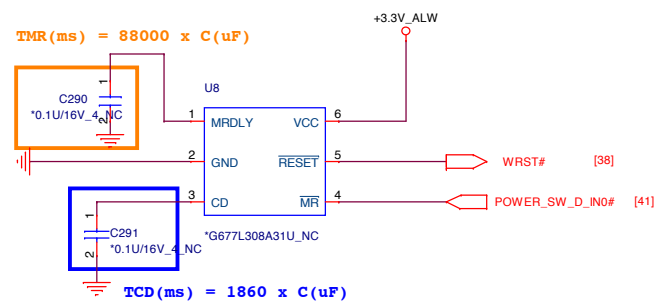


HDD access LED

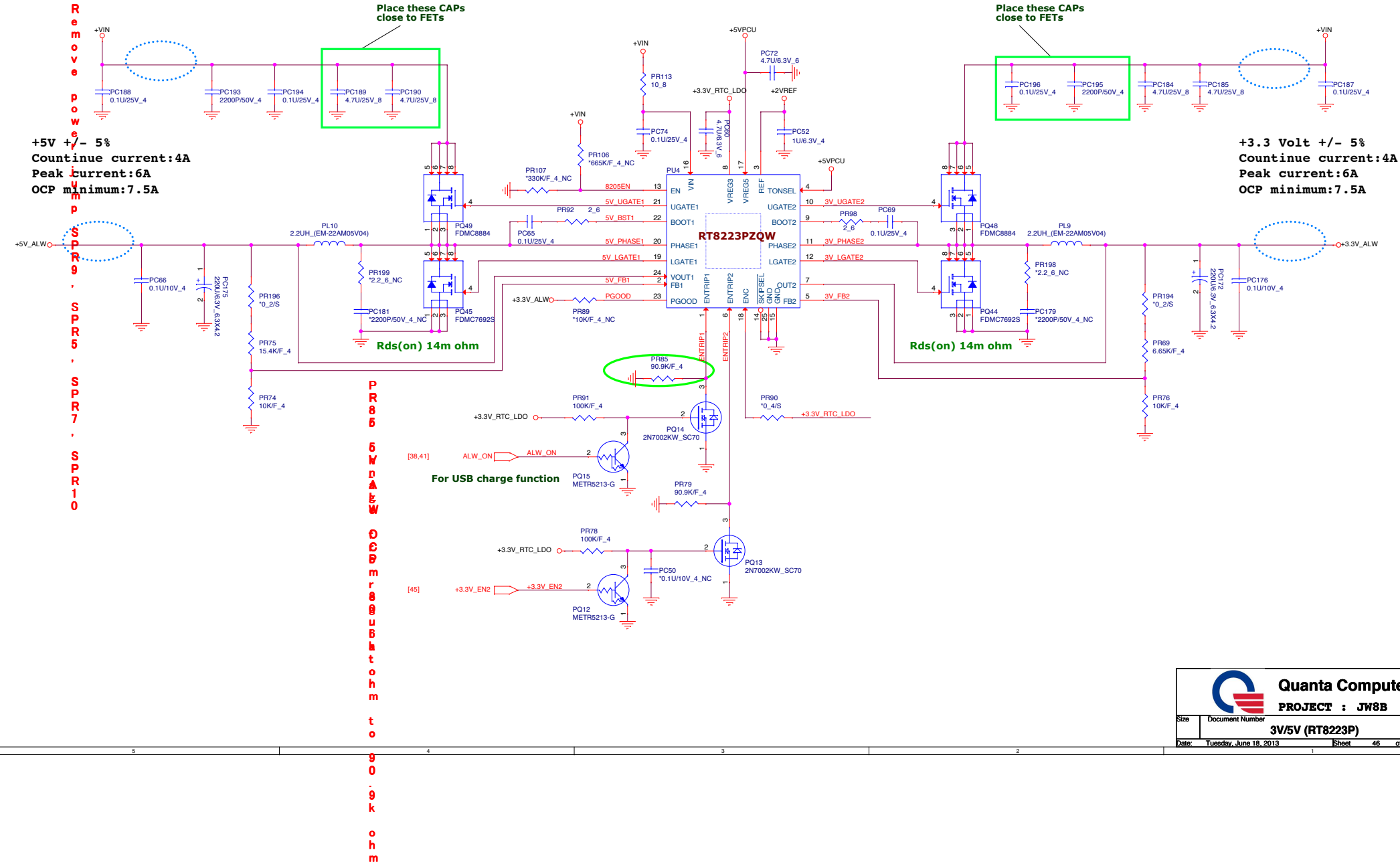




HW reset IC



DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

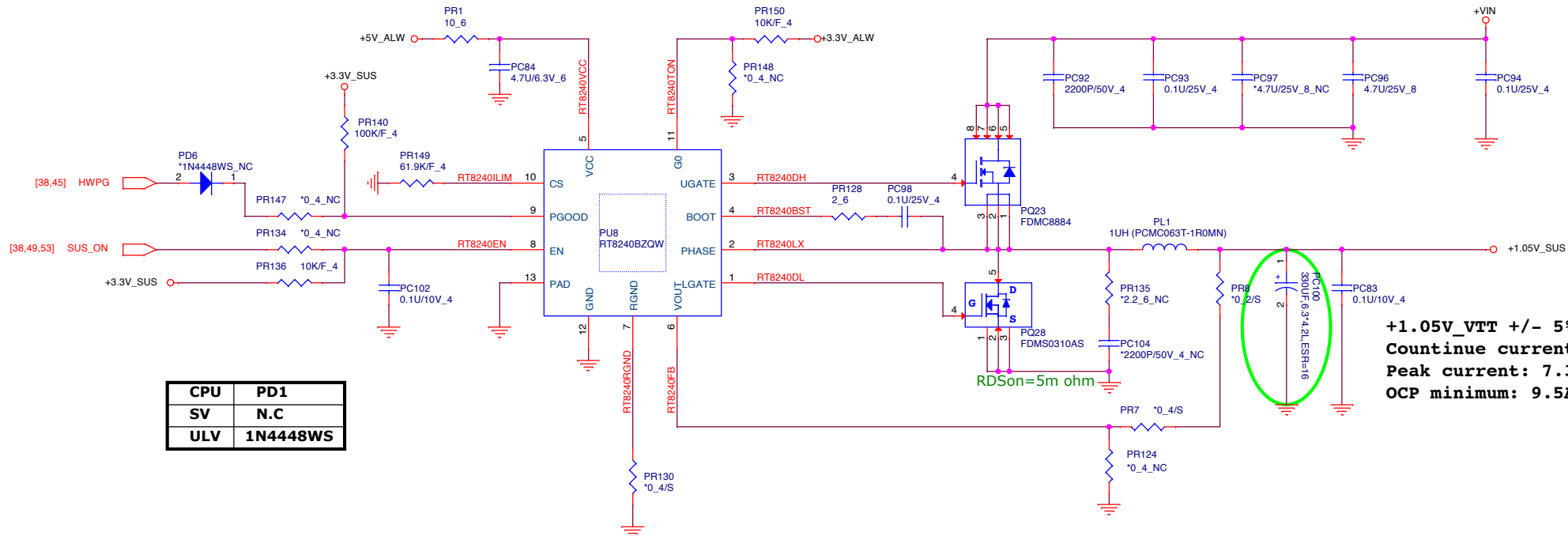


Adaptor protect circuit
 65W - 4.34A --> PR108 to 267k (CS42672FB16)
 90W - 5.62A --> PR108 to 137k (CS41372FB12)

Circuit-3

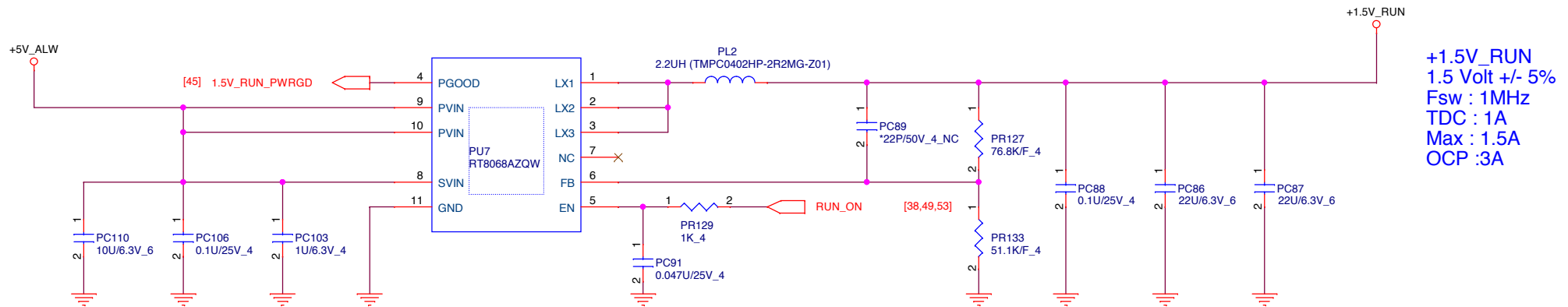
Circuit-1

Circuit-2



+1.05V_VTT +/- 5%
Countinue current: 5A
Peak current: 7.3A
OCp minimum: 9.5A

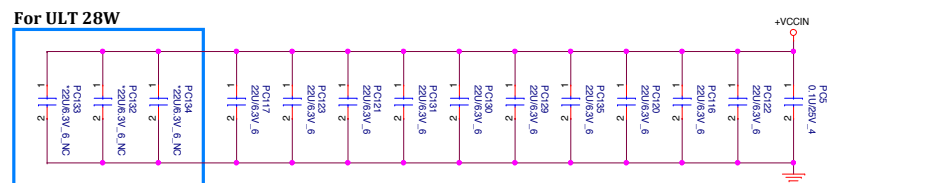
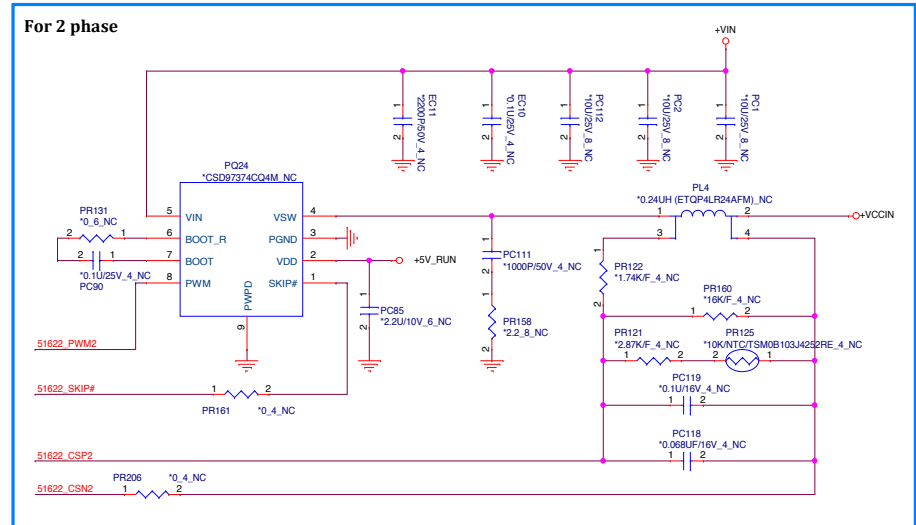
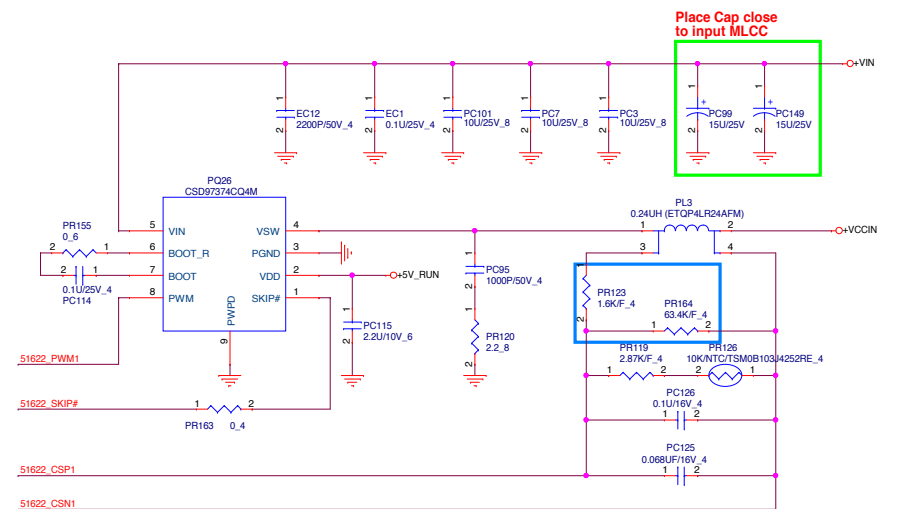
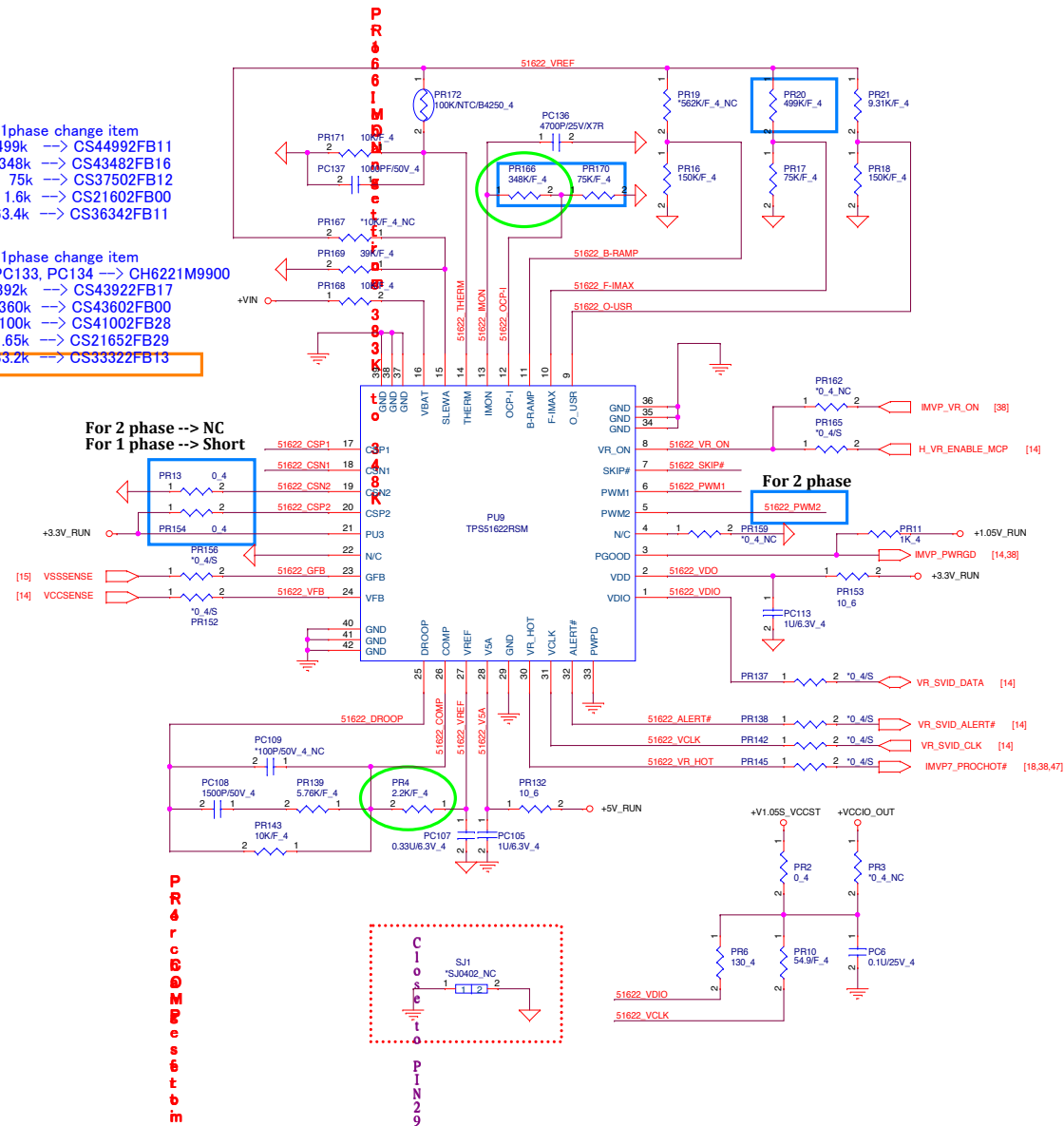
CPU	PD1
SV	N.C
ULV	1N4448WS

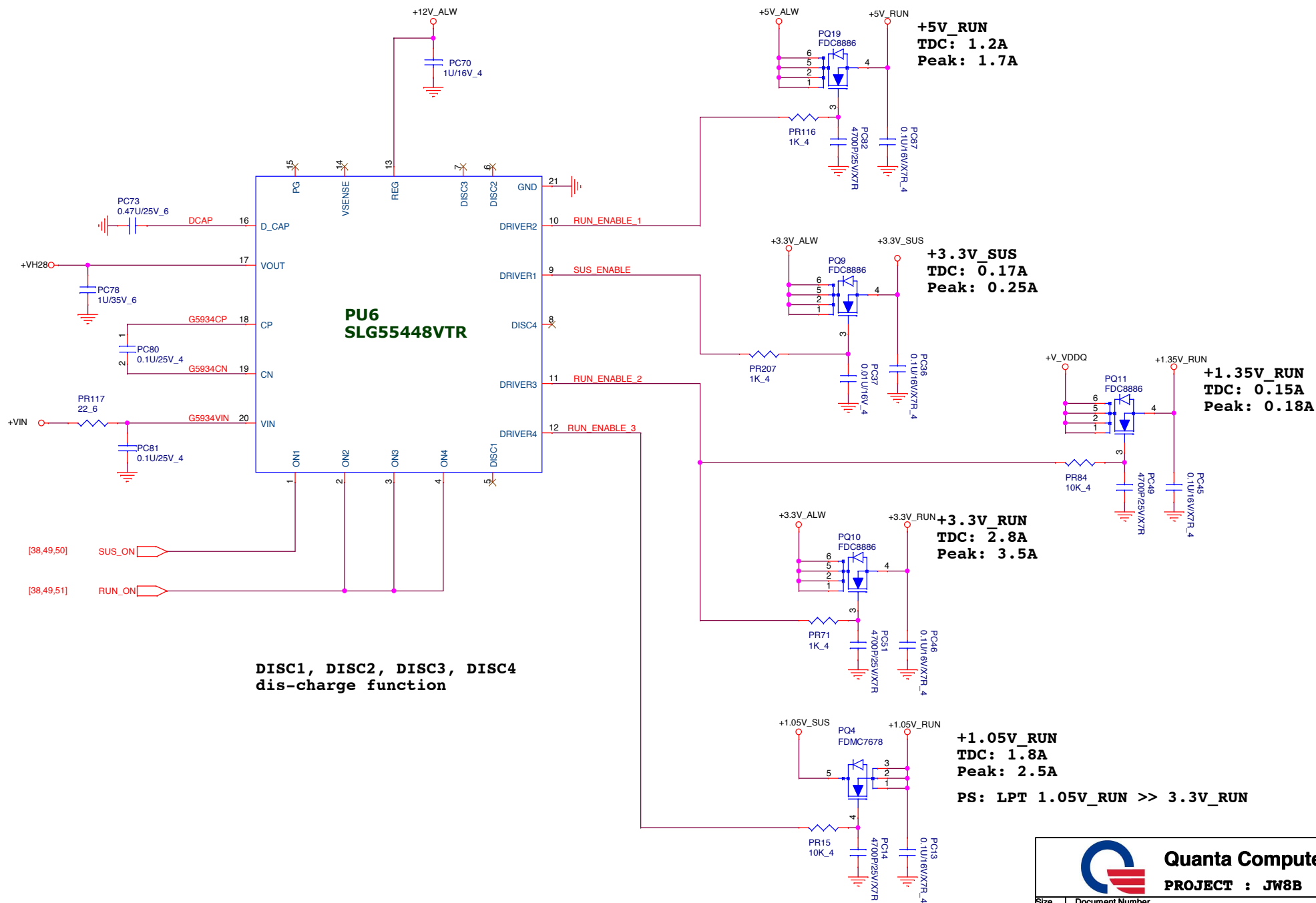


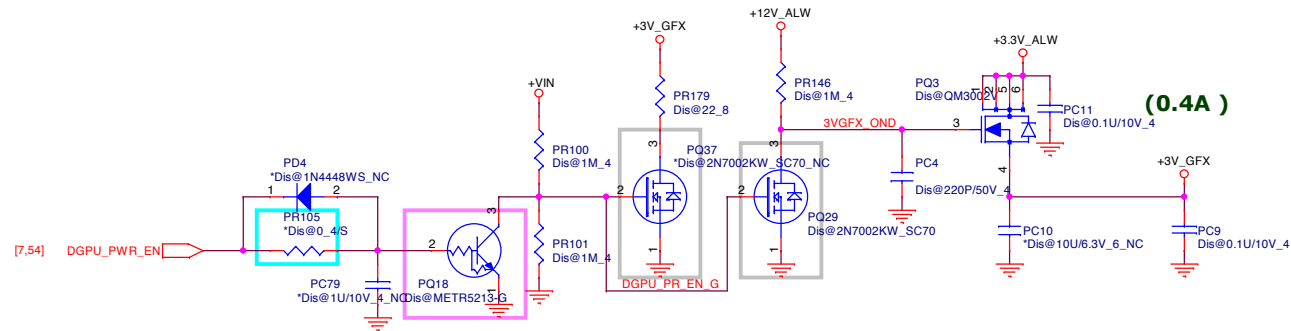
For 15W 1phase change item
 PR20 499k → CS44992FB11
 PR166 348k → CS43482FB16
 PR170 75k → CS37502FB12
 PR123 1.6k → CS21602FB00
 PR164 63.4k → CS36342FB11

For 28W 1phase change item
 PC132, PC133, PC134 → CH6221M9900
 PR20 392k → CS43922FB17
 PR166 360k → CS43602FB00
 PR170 100k → CS41002FB28
 PR123 1.65k → CS21652FB29
 PR164 33.2k → CS33322FB13

For 2 phase --> NC
 For 1 phase --> Short

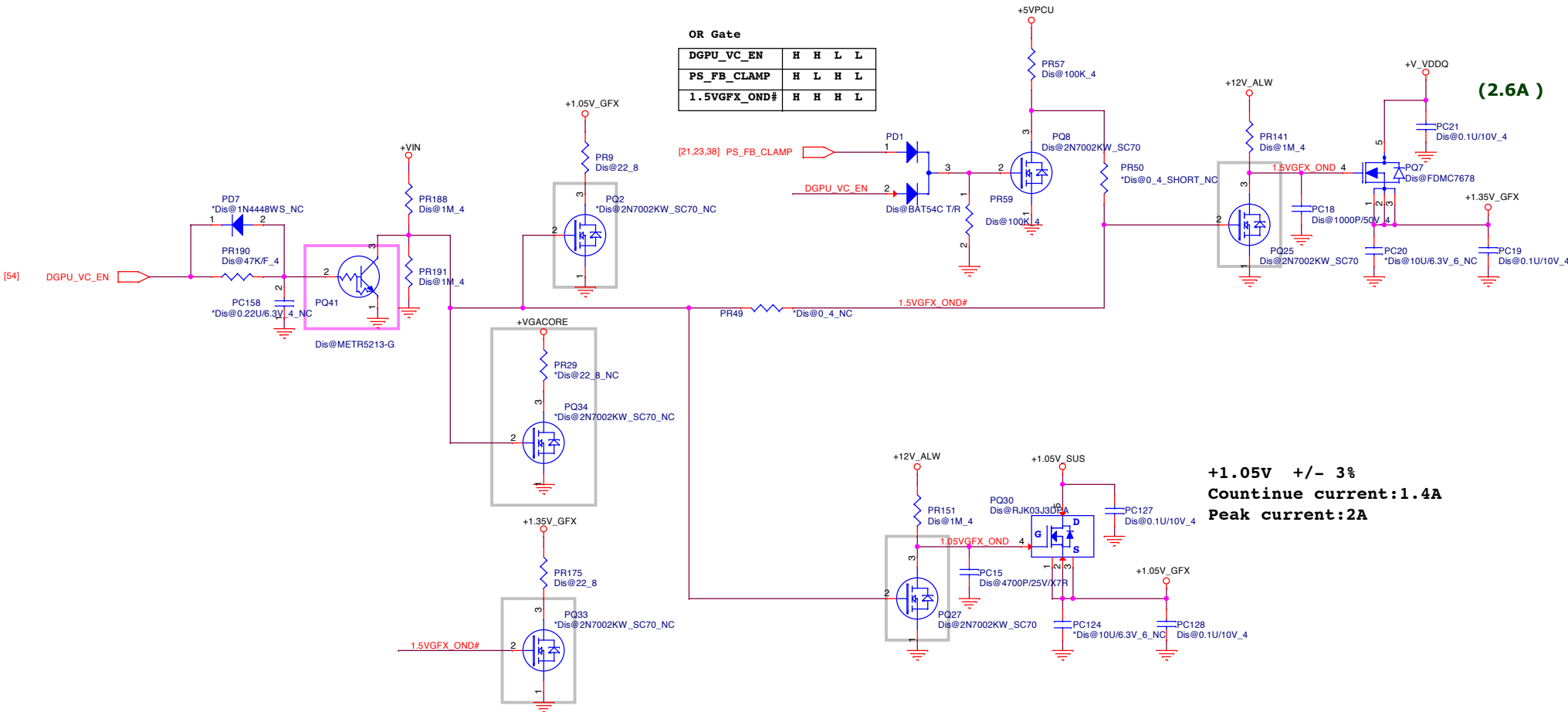






OR Gate

DGPU_VC_EN	H	H	L	L
PS_FB_CLAMP	H	L	H	L
1.5VGFEX_OND#	H	H	H	L



+1.05V +/- 3%
Countinue current:1.4A
Peak current:2A